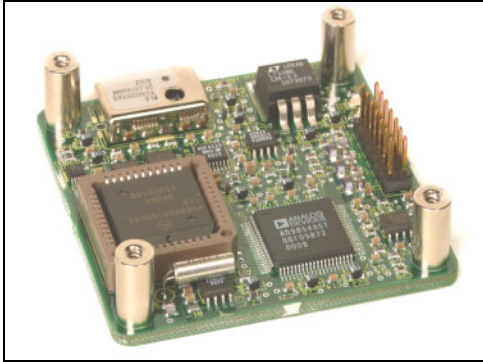


NOVATECH INSTRUMENTS, INC.

50MHz Locking Programmable Oscillator Model LPO30A



The LPO30A is a 50MHz Programmable Oscillator in a small modular package. The LPO30A generates a user programmable output signal up to 50MHz with 1 μ Hz resolution while locking to an external reference. The LPO30A is ideal for replacing long lead time custom frequency oscillators, allowing one master clock to be used throughout a system. When locked the accuracy and stability of the LPO30A will match that of the master. The lock frequency is programmable in 8kHz steps so the LPO30A can be locked to common telecom signals, such as T1, E1 and CDMA rates without external hardware, as well as laboratory standard frequencies of 10MHz and 5MHz. The LPO30A is ideal for applications which require distribution of a Stratum clock in embedded applications. The LPO30A can also be used without an external reference and delivers ± 2 ppm accuracy. An evaluation board is available for simplified testing and programming.

Specifications:

OUTPUT

TYPES: DC offset Sine.
IMPEDANCE: 100 Ω .
RANGE: 0Hz to 50MHz with 1 μ Hz resolution, 48-bits.
AMPLITUDE: 1V_{pp} \pm 0.25V_{pp} into 10k Ω , @1MHz, 12-bit resolution (4096 steps).

CONTROL

Settings are controlled through a bit-serial asynchronous I/O port (RS232 at TTL/CMOS level signals) at 19.2kBaud and can be saved in non-volatile memory.

ACCURACY AND STABILITY

Accuracy and stability depends upon customer supplied external clock. When locked, there is no fractional frequency error due to binary round-off.

EXTERNAL CLOCK IN

LEVEL: 0.5V_{rms} to 3V_{rms} Sine or Square Wave. 50 Ω .
FREQUENCY: 8kHz to 19.44MHz. The external lock frequency is programmable in 8kHz steps. The internal oscillator is phase locked to this value. Default: 10MHz.

TRACKING

The internal oscillator will track the externally supplied clock as long as the external frequency is within ± 5 ppm of the nominal value set for the external clock using the "Fr" command.

INTERNAL CLOCK MODE

The external lock can be disabled to use the internal oscillator for stand-alone operation with an accuracy of ± 1.5 ppm at 20 $^{\circ}$ C and a stability of ± 3 ppm from -20 to +60 $^{\circ}$ C. Other specifications are unchanged.

SPECTRAL PURITY (10k Ω load, 0.5V_{rms} 10MHz ref.)

Phase Noise: <-130dBc, 10kHz offset, 1MHz out.
Spurious: <-60dBc below 10MHz (50MHz span)
<-55dBc below 30MHz
<-45dBc below 50MHz
Harmonic: <-60dBc below 1MHz
<-55dBc below 10MHz
<-45dBc below 30MHz
<-35dBc below 50MHz

POWER REQUIREMENTS

+4.75 to +5.25 VDC @ <400mA

SIZE

60mm by 60mm square module. Max. height 13mm.

ENVIRONMENTAL

Temperature: -20 $^{\circ}$ C to +60 $^{\circ}$ C operating. Humidity: 80% to 31 $^{\circ}$ C, decreasing linearly to 50% at 40 $^{\circ}$ C.

CONNECTORS

14-pin Header (2x7 on a 2.54mm grid, 0.635mm square pins) contains all connections (see next page).

MOUNTING

Four #4-40 screws on 50.8mm square grid.

ACCESSORY

Model LPO30-EVAL board contains power supply, RS232 drivers, PC serial cable, buffer amplifier and BNC connectors for evaluation and programming of the LPO30A module. SOF8 software included.

22-Jan-2004

Serial Command	Function
F0 xx .xxxxxxxxxxxxxx	Set Frequency in MHz to nearest 1μHz. Decimal point required.
Fr xx .xxx	Sets the Reference Frequency in MHz in 8kHz steps. Decimal point required. Range: 8kHz to 19.44MHz. This value is used to phase lock the internal master clock to the externally supplied clock. Software rounds down to lowest 8kHz multiple.
P1 N	Set Phase. N is an integer from 0 to 16383. Phase is set to $N \cdot 360^\circ / 16384$ or $N \cdot \pi / 8192$ radians. Sets the relative phase of the output sine wave. This is useful for adjusting relative phase after the LPO30A has obtained lock.
Vi N	Set voltage level of output. N can range from 0 (off) to 4095 (no decimal point allowed). Voltage level is scaled to $N/4096$. If $N > 4095$, the scaling is turned off and the output is set to maximum. Increases power when used.
E x	Serial Echo Control. x=D for Echo D isable, x=E for Echo E nable. Default is E nabled.
S	Save current state into EEPROM and sets valid flag. State saved is used as default upon next power up or reset.
STOP	Turns off the internal microprocessor. The "STOP" command automatically saves all present settings. Use this command in embedded applications for lowest system noise and power. A logic low (open collector) pulse must be applied to the CLR_STOP* connector pin to restore normal operation. After a CLR_STOP* pulse, factory defaults are restored.
R	Reset. This command resets the unit. EEPROM data is preserved and, if valid, it is used upon restart. This is the same as cycling power or toggling the open collector RES* line on the connector.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
QUE	Read present frequency, phase and status. Returns an 42-character string of internal settings, lock status and software revision number. Hexadecimal format.
C x	E nable (x=E) or D isable (x=D) external lock. When disabled, the internal TCXO is used without locking to the externally supplied clock.

Pin Number	Function	Type	Pin Number	Function	Type
1	Ground (Power Supply Common)	PS	2	RF_OUT, Synthesized Signal Output, 100Ω. DC offset sine.	Out
3	TX, serial ASCII data FROM module, TTL level (3.3 V CMOS)	Out	4	Ground (Power Supply Common)	PS
5	+5.0 V (+4.75 to +5.25V)	PS	6	RX, serial ASCII data TO module, TTL level (3.3 V CMOS)	In
7	+3.3 V (from on-board regulator). 50mA MAX.	PS	8	RES*, Open Collector Reset Pin, normally left open.	In
9	Ground (Power Supply Common)	PS	10	CLR_STOP*, Open Collector Input Pin. Pulsing low clears module to factory defaults.	In
11	INLOCK (TTL level, 3.3 V CMOS), 500Ω source resistance.	Out	12	Ground (Power Supply Common)	PS
13	RF_IN, Reference Clock Input, 50Ω.	In	14	Ground (Power Supply Common)	PS

Operating Notes for assembly POM30/LPO30 and LPO30A, with REV x.x Software.

(January 22, 2004)

1: The 'QUE' command has been rewritten to provide data specific to the POM30/LPO30/LPO30A. The command returns a forty-two character ASCII string terminated by a CRLF:

```
0000 12309ce54000 2710 14050040 0fff 03 20
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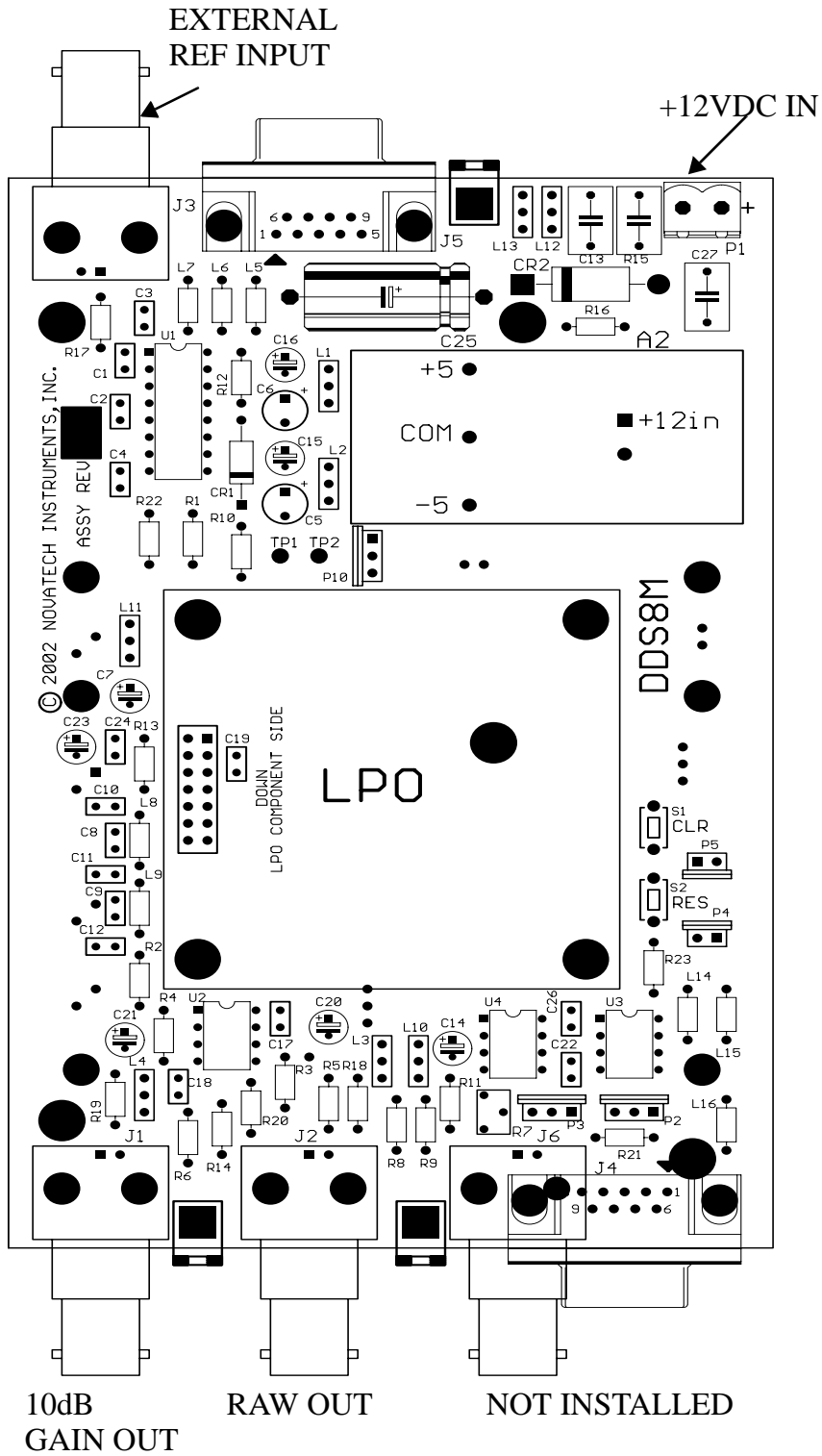
Decoding:

0000	Relative phase in Hex. Maximum value of '3fff'. Set by P1 command.
12309CE54000	48-bit Frequency data (6-bytes). This value is the frequency in 0.5µHz steps. It is multiplied by 2 to obtain output frequency. 10.0MHz default value.
2710	Reference frequency set by 'Fr' command. Software sets to lowest 8kHz boundary. Saved as a hex value as kHz. 10000 (as Hexadecimal), for 10MHz reference frequency, default.
14050040	Control Register values. These are internal setup values.
0FFF	Value of output DAC multiplier. Set by 'Vi' command. Default is multiplier off and set to '0FFF'.
03	This byte contains status bits. The LSB is the lock bit. If an out-of-lock condition is detected, the bit will go low (even). '03' means that the POM30/LPO30 has been locked. The microprocessor reads the lock pin every millisecond and sets this value low upon detection of a out-of-lock.
20	Software revision as 'x.x' or Rev 2.0 for this example.

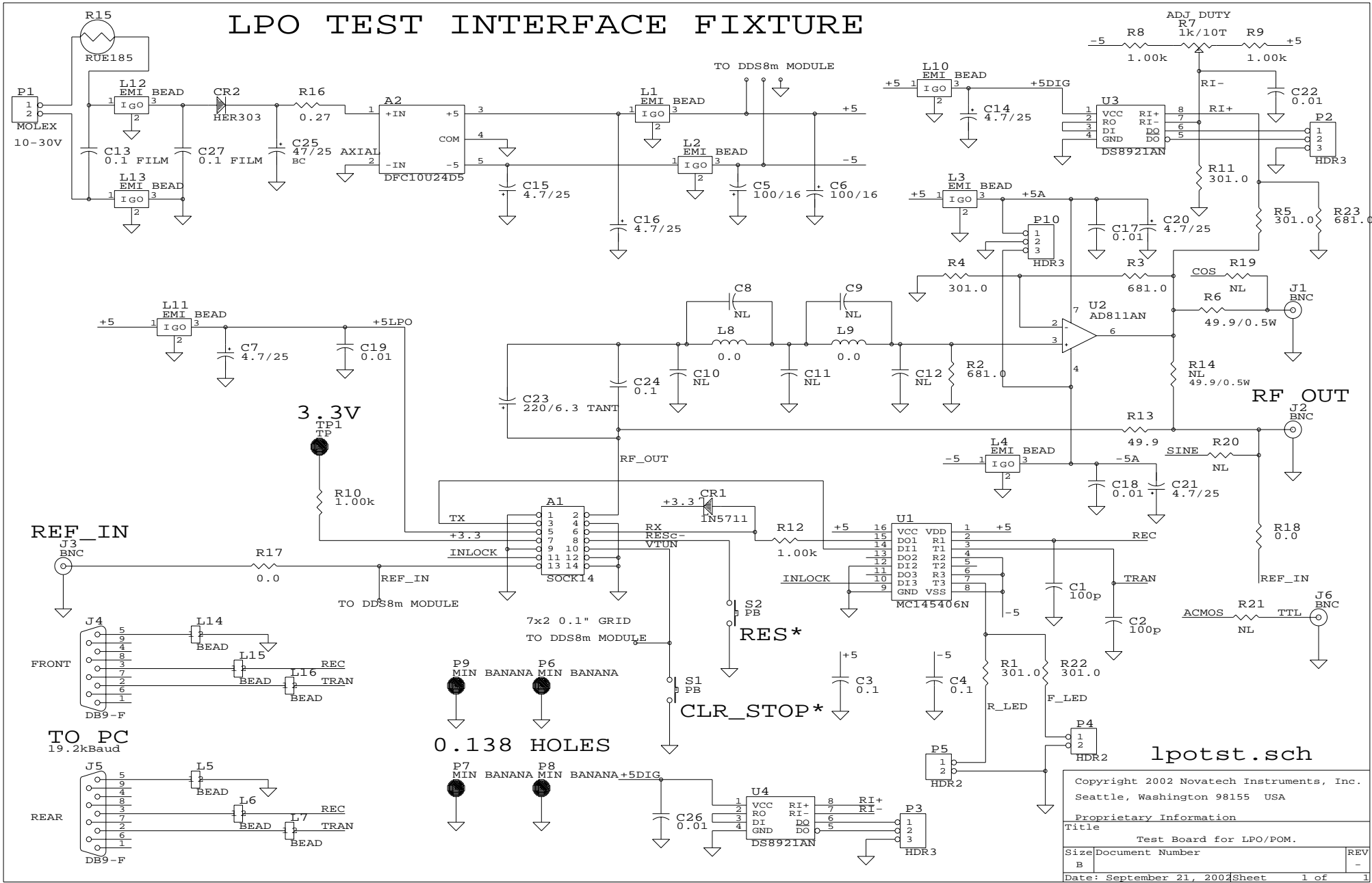
2: The InLock Pin on the interface connector, pin 11 of P1, will be steady logic low during lock. During the locking process, this pin will be erratic. It is suggested that, if you use this pin, it be polled. The on-board microprocessor reads the lock status each millisecond, for example. The lock detect process cannot detect minor changes in the reference input or the lock frequency setting.

3: Commands return 'OK' if parsed and executed correctly.

4: Green is "Lock" and Red is "Out-of-Lock." If both LEDs are glowing then the circuit is in a transition/acquisition phase.



LPO TEST INTERFACE FIXTURE



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Title Test Board for LPO/POM.		
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