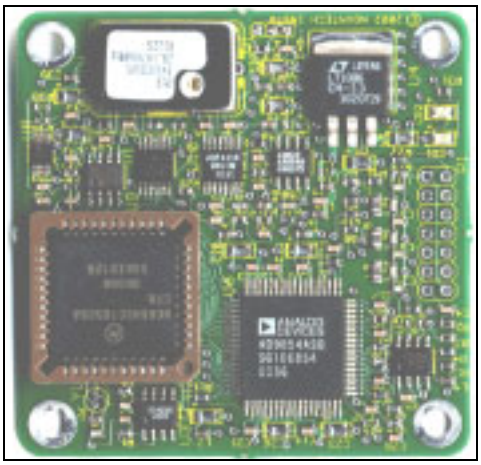
NOVATECH
INSTRUMENTS, INC.

40MHz Locking Programmable Oscillator

Model LPO30A



The LPO30 is a 40MHz Programmable Oscillator in a small modular package. The LPO30 generates a user programmable output signal up to 40MHz with 1μHz resolution. The LPO30 is ideal for replacing long lead time custom frequency oscillators, allowing one master clock to be used throughout a system. The accuracy and stability of the LPO30 will match that of the master. The lock frequency is programmable in 8kHz steps so the LPO30 can be locked to common telecom signals, such as T1 and E1 rates without external hardware. The LPO30 is ideal for applications which require distribution of a Stratum clock in embedded applications. An evaluation kit is available for simplified testing and programming.

Specifications:

OUTPUT
TYPES: DC offset Sine.
IMPEDANCE: 100Ω.
RANGE: 1μHz to 40MHz with 1μHz resolution, 48-bits.
AMPLITUDE: 12-bit resolution (4096 steps), 1Vpp ±0.25Vpp into 10kΩ.

CONTROL
Settings are controlled through a bit-serial asynchronous I/O port (RS232 at TTL/CMOS level signals) at 19.2kBaud and can be saved in non-volatile memory.

ACCURACY AND STABILITY
Accuracy and stability depends upon customer supplied external clock. When locked, there is no fractional frequency error due to binary round-off.

EXTERNAL CLOCK IN
LEVEL: 0.5V_{rms} to 3V_{rms} Sine or Square Wave. 50Ω.
FREQUENCY: 8kHz to 19.44MHz. The external lock frequency is programmable in 8kHz steps. The internal oscillator is phase locked to this value. Default: 10MHz.

TRACKING
The internal oscillator will track the externally supplied clock as long as the external frequency is within ±5ppm of the nominal value set for the external clock using the "Fr" command.

INTERNAL CLOCK MODE
The external lock can be disabled to use the internal oscillator for stand-alone operation. This clock has a accuracy of ±1.5ppm at 20°C and a stability of ±3ppm from -20 to +60°C. Other specifications are unchanged.

SPECTRAL PURITY (10kΩ load, 0.5V_{rms} 10MHz ref.)

Phase Noise:	<-140dBc, 10kHz offset, 1MHz out.
Spurious:	<-60dBc below 10MHz (20MHz span)
	<-55dBc below 30MHz
	<-50dBc below 40MHz
Harmonic:	<-60dBc below 1MHz
	<-55dBc below 10MHz
	<-45dBc below 30MHz
	<-40dBc below 40MHz

POWER REQUIREMENTS
+4.75 to +5.25 VDC @<400mA

SIZE
60mm by 60mm square module. Max. height 13mm.

ENVIRONMENTAL
Temperature: -20°C to +60°C operating. Humidity: 80% to 31°C, decreasing linearly to 50% at 40°C.

CONNECTORS
14-pin Header (2x7 on a 2.54mm grid, 0.635mm square pins) contains all connections (see next page).

MOUNTING
Four #4-40 screws on 50.8mm square grid.

ACCESSORY
Model LPO30-EVAL board contains power supply, RS232 drivers, PC serial cable, buffer amplifier and BNC connectors for evaluation and programming of the LPO30A module.

21-Jan-2003

NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America
http://www.novatech-instr.com/
sales@novatech-instr.com
206.363.4367 FAX/206.301.8986 Voice

Serial Command	Function
F0 xx.xxxxxxxxxxx	Set Frequency in MHz to nearest 1μHz. Decimal point required.
Fr xx.xxx	Sets the Reference Frequency in MHz in 8kHz steps. Decimal point required. Range: 8kHz to 19.44MHz. This value is used to phase lock the internal master clock to the externally supplied clock. Software rounds down to lowest 8kHz multiple.
P1 N	Set Phase. N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*π/8192 radians. Sets the relative phase of the output sine wave. This is useful for adjusting relative phase after the LPO30 has obtained lock.
Vi N	Set voltage level of output. N can range from 0 (off) to 4095 (no decimal point allowed). Voltage level is scaled to N/4096. If N >4095, the scaling is turned off and the output is set to maximum. Increases power when used.
E x	Serial Echo Control. x=D for Echo **D**isable, x=E for Echo **E**nable. Default is **E**nabled.
S	Save current state into EEPROM and sets valid flag. State saved is used as default upon next power up or reset.
STOP	Turns off the internal microprocessor. The "STOP" command automatically saves all present settings. Use this command in embedded applications for lowest system noise and power. A logic low (open collector) pulse must be applied to the CLR_STOP* connector pin to restore normal operation. After a CLR_STOP* pulse, factory defaults are restored.
R	Reset. This command resets the unit. EEPROM data is preserved and, if valid, it is used upon restart. This is the same as cycling power or toggling the open collector RES* line on the connector.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
QUE	Read present frequency, phase and status. Returns an 42-character string of internal settings, lock status and software revision number. Hexadecimal format.
C x	**E**nable (x=E) or **D**isable (x=D) external lock. When disabled, the internal TCXO is used without locking to the externally supplied clock.

Pin Number	Function	Type	Pin Number	Function	Type
1	Ground (Power Supply Common)	PS	2	RF_OUT, Synthesized Signal Output, 100Ω. DC offset sine.	Out
3	TX, serial ASCII data FROM module, TTL level (3.3 V CMOS)	Out	4	Ground (Power Supply Common)	PS
5	+5.0 V (+4.75 to +5.25V)	PS	6	RX, serial ASCII data TO module, TTL level (3.3 V CMOS)	In
7	+3.3 V (from on-board regulator). 50mA MAX.	PS	8	RES*, Open Collector Reset Pin, normally left open.	In
9	Ground (Power Supply Common)	PS	10	CLR_STOP*, Open Collector Input Pin. Pulsing low clears module to factory defaults.	In
11	INLOCK (TTL level, 3.3 V CMOS), 500Ω source resistance.	Out	12	Ground (Power Supply Common)	PS
13	RF_IN, Reference Clock Input, 50Ω.	In	14	Ground (Power Supply Common)	PS