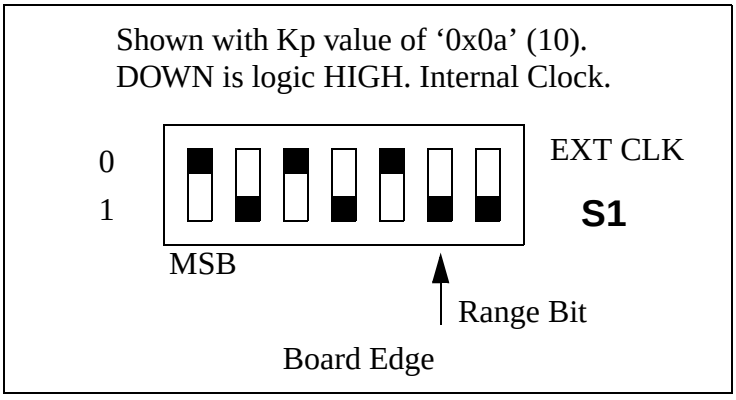
Addendum to DDS8p operating instructions.

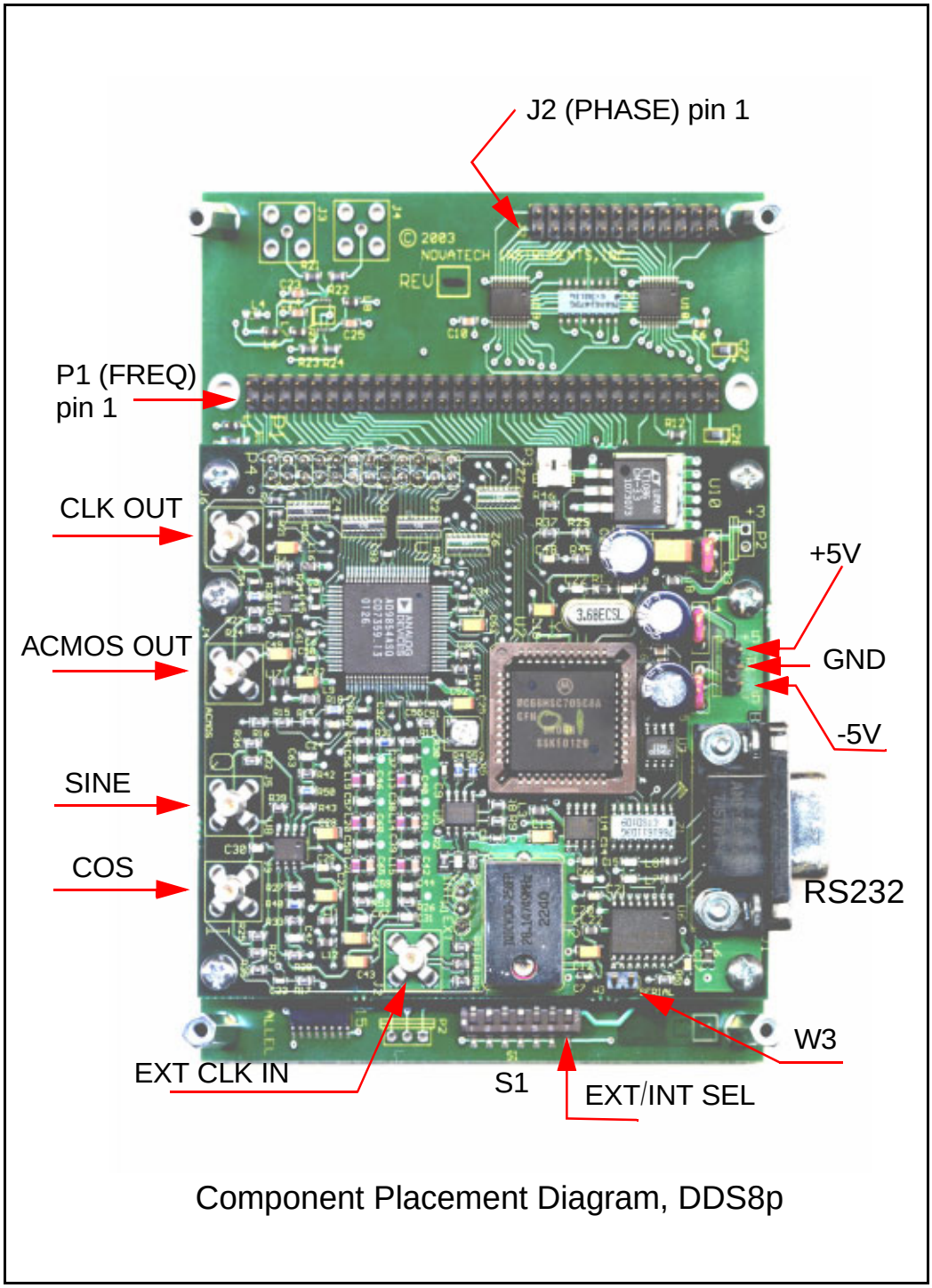
The model DDS8p has a dip switch which is used to set the value of Kp (overrides software set value), to set the internal PLL range bit, and to select internal or external clock.

The value of Kp is 5-bits binary, with legal values of 4 to 20. (The maximum internal clock frequency, Kp times External Reference Frequency, is 300MHz). The first five left-most positions of switch S1 are used to set this value. Note that logical one is down in this figure (near the board edge on the actual DDS8p). The range bit should be set high for master clocks (reference clock frequency multiplied by Kp) of 200-300MHz (default is high). It should be set low for master clocks less than 200MHz.

The right-most switch position selects the clock source. As shown, the internal reference clock source (approximately 28.147MHz) is selected. If moved to the up position (logic zero), the customer supplied external reference clock is used. This switch is always active.

The values of Kp and the range bit are only read upon power up or after a reset.





Component Placement Diagram, DDS8p