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re: Byte Parallel initialization for DDS8m board.

NOTE: The signals on the dds8m require 3.3 volt CMOS logic levels: 5 volt levels will damage the board.

The DDS8m has 40 registers (addresses 0x00 to 0x27) which must be initialized for correct operation. The easiest and most straightforward way of performing this initialization is to store default register values in the host software and send each value byte-by-byte. Output values can then be sent as necessary, with most of the registers remaining unchanged in normal operation.

Some points are important to note. The on-board DDS chip defaults to source the master IOUD (I/O UpDate) signal. Until this is changed to an input, the bus timing is set by this signal. Novatech Instruments, Inc. software starts with an “OWN_IOUD” control routine. Also, until all the registers are initialized the state of the output will be undetermined.

The values in the registers are determined by the mode you wish to be the default for your application. The values shown below are for a frequency multiplier of 10, Mode 1 (FSK), External IOUD, Q-channel off, amplitude multipliers off, Sinc filter off. The example shown is in Motorola 68HC05 assembly code, but this can be considered to be “pseudo-code” for any processor or higher level language.

```
*********define all ROM constants eprom data here*********
* the default dds8m registers must be here and in the same order
* (and count) as in the AD9854.  Upon initialization data will be read from
* here and loaded into the dds8m. Names are abbreviated from the Data Sheet.

      def_PAR1    fcb $00,$00
      def_PAR2    fcb $00,$00
      def_FTW1    fcb $00,$00,$00,$00,$00,$00 ;zero hertz
      def_FTW2    fcb $09,$18,$4e,$72,$a0,$00  ;10MHz MSB first (lowest addr)
      def_DFW     fcb $00,$00,$00,$00,$00,$00
      def_UC      fcb $00,$00,$00,$05  ;IOUD time
      def_RRC     fcb $00,$00,$00
      def_CR3     fcb %00000010 ;comparator on, qdac off, dig on, dacs on
      def_CR2     fcb %01001010 ;pll on, x10, high gain
```

```
def_CR1     fcb %00000010 ;mode 1, external IOUD
def_CR0     fcb %01000000 ;inv sinc bypassed
def_OSKI    fdb $0fff
def_OSKQ    fdb $0fff
def_OSKRR   fcb $00
def_QDAC    fdb $0fff
def_AMP     fdb $0fff ;max amp
def_MODE    fcb $02 ;default mode is FSK with FSK-pin high for FTW2 out.
```

The pseudo code “fcb” means “fixed constant byte” (8 bits) and “fdb” means “fixed double byte” (16 bits). The addresses are shown from 0x00 to 0x27. The “def_” prefix on the register abbreviation refers to the “default” values to be stored.

The “OWN_IOUD” routine simply writes to the Control Registers (CR3 through CR0) in reverse order, waiting 1ms between each write. After all registers are written, the host IOUD pin is changed to an output and is pulsed to ensure loading of the correct values. This routine is run before the list of registers above is written.

See the Model DDS8m manual for the registers.

Note that when the DDS8m is used in byte-parallel the operation of the board is completely dependent upon the host software. The OEM’s test procedure on the final application must test all applicable functions. It is suggested that you study the data sheet for the AD9854 used on board (http://www.analog.com) for further operational details.