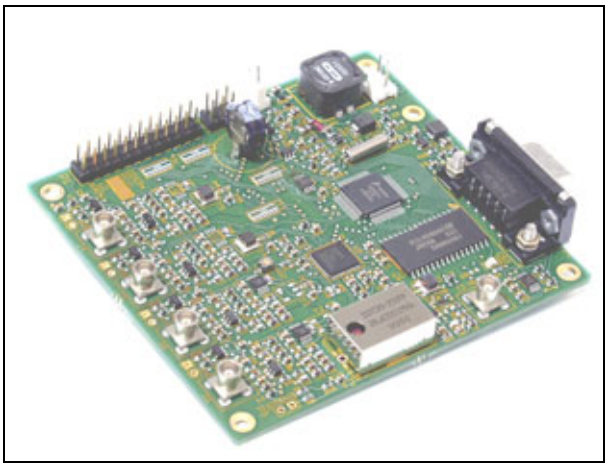
NOVATECH
INSTRUMENTS, INC.

170MHz Four Channel Signal Generator Module

Model DDS9m



The DDS9m is a 170MHz Four Channel Direct Digital Synthesized Signal Generator on a small circuit board module. The DDS9m generates four Sine and four LVCMOS output signals simultaneously up to 170MHz in 0.1Hz steps under RS232 control. The frequencies of the four outputs can be set independently and can be offset by a controllable phase, with independent amplitudes. The RS232 interface uses simple text commands to control the module and allows non-volatile storage of all settings. The DDS9m is equipped with a ±1.5ppm on-board VCTCXO clock and can accept an external clock source up to 500MHz. Up to 32k points can be stored in the Table Mode for arbitrary phase, amplitude and frequency profiles.

Specifications:

OUTPUTS
TYPES: Four Sine and LVCMOS simultaneously (four frequencies.)
IMPEDANCE: Sine: 50Ω; LVCMOS: 50Ω.
RANGE: 0.1Hz to 171MHz in 0.1Hz steps (int. clock).
SINE AMPLITUDE: approximately $1V_{pp}$ (+4dBm) into 50Ω. Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits), or by scale factors of 1/2, 1/4, or 1/8.
PHASE: Each channel 14-bits programmable.
FLATNESS: ±3dB from 1kHz to 150MHz referenced to amplitude at 35MHz, full scale.

LVCMOS AMPLITUDE
V_{oh} >=2.4V and V_{ol} <=0.4V when series terminated. Rise and fall times <1.5ns with <15pF load. (>1MHz, <125MHz)

CONTROL
Output frequencies, amplitudes (10-bits) and phases (14-bits) are controlled by an RS232 serial port at 19.2kbaud. All settings (except table mode data) can be saved in non-volatile (EEPROM) memory via the RS232 port.

ACCURACY AND STABILITY
Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±1ppm per year, 18 to 28°C. (Internal Clock)

EXTERNAL CLOCK IN
LEVEL: 0.2 to $0.5V_{rms}$ Sine or Square Wave. 50Ω.
FREQUENCY: 10MHz to 125MHz with multiplier of 4 to 20 enabled. Direct input of 1MHz to 500MHz.

SPECTRAL PURITY (Typ. 50Ω load, internal clock, full-scale output)
Phase Noise: <-120dBc, 10kHz offset, 5MHz out.
Spurious: <-60dBc below 10MHz (typ. 300MHz span)
<-60dBc below 40MHz
<-55dBc below 80MHz
<-50dBc below 160MHz
Harmonic: <-65dBc below 1MHz
<-55dBc below 20MHz
<-45dBc below 80MHz
<-35dBc below 160MHz
(channel-channel isolation: <-60dBc)

TABLE MODE
On-board 4Mb static ram holds up to 32,768 profile points in table mode allowing a different output in 100µs increments.

POWER REQUIREMENTS
+3.14V to +3.46VDC@<750mA. Battery back-up 3.0V at <400µA (2-AA, LR6, typical, customer supplied).

SIZE
82.6mm by 88.9mm circuit board. Max. height 10mm.

CONNECTORS
MCX (SMA optional) for Sine Outputs and EXT CLK IN. 2-pin header for +3.3V power and external back-up battery. 24-pin header for high speed control. DE9 for Serial Control. 2-pin wirepoints for LVCMOS.

3-May-2011

NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America
http://www.novatech-instr.com/
sales@novatech-instr.com
206.363.4367 FAX, 206.301.8986 Voice

Table 2: RS232 Serial Commands

RS232 Command	Function
`Fn xxx.xxxxxxx`	Set Frequency of output "n" in MHz to nearest 0.1Hz. Decimal point required. n=0, 1, 2, 3. Maximum setting: 171.1276031MHz. Single tone mode.
`Pn N`	Set Phase of output "n." N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*π/8192 radians. Sets the relative phase of the frequency output depending upon the value of n=0, 1, 2, 3. Single tone mode.
`E x`	Serial echo control. x=D for Echo **D**isable, x=E for Echo **E**nable
`C x`	Select clock source. x=E for **E**xternal clock, x=I for **I**nternal Clock. May require adjustment of Kp and external filtering of output.
`R`	Reset. This command resets the DDS9m. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
`CLR`	Clear. This command clears the EEPROM valid flag and restores all factory default values.
`A x`	x=E for LVCMOS **E**nable, x=D for LVCMOS **D**isable.
`S`	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the `"CLR"` command to return to default values.
`QUE`	Return present frequency, phase and status. Returns a character string of all internal settings.
`M N`	Mode command. Mode '0' is single tone on all channels (default). If N=a, then the phase is automatically cleared during each command ; if N=n, then the phase is not cleared (default). See manual for details.
`Vn N`	Set voltage level of output "n." In default, the amplitude is set to the maximum: approximately 1V_{pp} (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1023. n=0, 1, 2, 3 to set the amplitude on frequency 0, 1, 2 or 3. If N >=1024, the scaling is turned off and the selected output is set to full scale.
`Vs N`	Set the output scaling factor. N=1 for fullscale, N=2 for half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
`Kp aa`	Set PLL reference multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01_h, 04_h to 14_h). Values of Kp times clock frequency must not be between 160MHz and 255MHz (for internal clock, this disallows 5<=Kp<= 9).
`I x`	Set the I/O update pulse method. If x=a, then an I/O update is issued **a**utomatically at the end of each serial command (default). If x=m, then a **m**anual I/O update pulse is expected to be sent by a subsequent `'I p'` command.
B aa[bb[cc[dd[ee[ff[gg]]]]]]	This **B**yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the function. Please consult the manual for details. Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed. See manual for details.

Table Mode Details.

The Model DDS9m contains an on-board static RAM capable of storing up to 32,768 profile points for Channels 0 and 1. Each point contains phase, frequency, amplitude and dwell time information. The on-board microcomputer reads this RAM and programs the DDS ASIC per the profile point data. The profile can be set to loop continuously or to hold at the last point, until interrupted by a subsequent command. The table mode is toggled on and off by an `'M t'` command from the serial port and executes customer provided profile points. `'M 0'` always turns off the table and returns to single tone mode. The DDS9m starts execution of the profile immediately upon a receipt of `'M t'` following an `'M 0'`.

NOTE:

The table mode or table RAM is not accessible from the high speed port. The high speed port controls only the DDS ASIC.

The command sequence is of this form (comments after the ';' are not sent to the DDS9m, but are here for explanation purposes):

```
M 0                                 ;turns off running table mode
t0 0000 aabbccdd,eeff,gghh,ii       ;F0 profile point 0
t1 0000 aabbccdd,eeff,gghh,ii       ;F1 profile point 0
t0 0001 aabbccdd,eeff,gghh,ii       ;F0 profile point 1
t1 0001 aabbccdd,eeff,gghh,ii       ;F1 profile point 1
...
t0 3fff aabbccdd,eeff,gghh,ii       ;F0 profile point 0x3fff
t1 3fff aabbccdd,eeff,gghh,ii       ;F1 profile point 0x3fff
M t                                 ;begin execution of table
```

;`'0000'` two byte RAM address, T0 and T1 must be paired with same address
;`'aabbccdd'` four bytes frequency, hexadecimal, MSB first, 4 bytes. 0.1Hz resolution on LSB
;`'eeff'` phase offset, hexadecimal, MSB first, only 14-bits active, top two bits are ignored
;`'gghh'` amplitude scale, MSB first, only 10-bits active. Amplitude is scaled per above.
;`'ii'` dwell time, MSB first, in increments of 100µs. 0x00=loop back to start, 0xff=hold present setting. Each T0:T1 pair must have the same dwell.

The `','` (comma) in each record is used as a delimiter and must be included as shown. The inputs are are not case sensitive. Subsequent `'M t'` commands will toggle the execution of the table on and off. Upon execution of the table, the output will always begin with address 0000 and progress until it encounters an 0xff or 0x00 in a dwell position. The last record in a table mode will be executed for 100µs if the dwell is set to 00.

The current values stored in RAM can be read back by the `"Dn aaaa"` command. N=0 or 1 and "aaaa" is the address.

The RAM table is backed-up by a "supercap" for a minimum of 10 minutes. Provision is provided for a customer supplied 3V battery, typically two LR6 (AA) batteries. Ten minutes provides ample time for battery replacement, which will hold the RAM data for approximately one year with no power applied to the DDS9m.