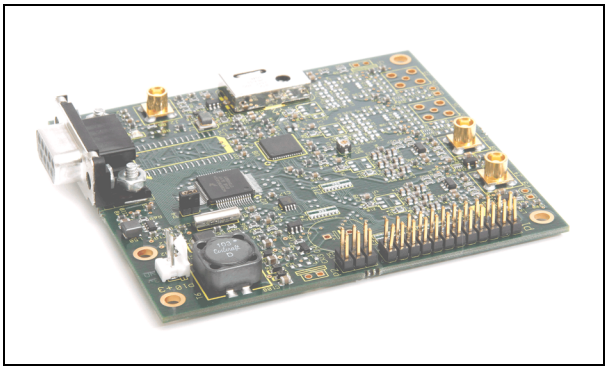
NOVATECH
INSTRUMENTS, INC.

171MHz Two Channel Signal Generator Module
Model DDS9m/02



The DDS9m/02 is a 171 MHz two Channel Direct Digital Synthesized Signal Generator on a small circuit board module. The DDS9m/02 generates two Sine and two LVCMOS output signals simultaneously up to 171 MHz in 0.1 Hz steps under RS232 control. The frequencies of the two outputs can be set independently and can be offset by a controllable phase, with independent amplitudes. The RS232 interface uses simple text commands to control the module and allows non-volatile storage of all settings. The DDS9m/02 is equipped with a ±1.5ppm on-board VCTCXO clock and can accept an external clock source up to 500 MHz.

Specifications:

OUTPUTS
TYPES: Two Sine and LVCMOS simultaneously (two frequencies.)
IMPEDANCE: Sine: 50Ω; LVCMOS: 50Ω.
RANGE: 0.1 Hz to 171 MHz in 0.1Hz steps (int. clock).
SINE AMPLITUDE: approximately $1V_{pp}$ (+4dBm) into 50Ω. Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits), or by scale factors of 1/2, 1/4, or 1/8.
PHASE: Each channel 14-bits programmable.
FLATNESS: ±3dB from 1 kHz to 150 MHz referenced to amplitude at 35 MHz, full scale.

LVCMOS AMPLITUDE
V_{oh} >=2.4V and V_{ol} <=0.4V when series terminated. Rise and fall times <1.5ns with <15pF load. (>1MHz, <125MHz)

CONTROL
Output frequencies, amplitudes (10-bits) and phases (14-bits) are controlled by an RS232 serial port at 19.2kbaud, or direct connection to the DDS generator. All settings can be saved in non-volatile (EEPROM) memory via the RS232 port.

ACCURACY AND STABILITY
Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±1ppm per year, 18 to 28°C. (Internal Clock)

EXTERNAL CLOCK IN
LEVEL: 0.2 to 0.5 V_{rms} Sine or Square Wave. 50Ω.
FREQUENCY: 10 MHz to 125 MHz with multiplier of 4 to 20 enabled. Direct input of 1 MHz to 500 MHz.

SPECTRAL PURITY (Typ. 50Ω load, internal clock, full-scale output)
Phase Noise: <-120dBc, 10kHz offset, 5 MHz out.
Spurious: <-60dBc below 10 MHz (typ. 300 MHz span)
<-60dBc below 40 MHz
<-55dBc below 80 MHz
<-50dBc below 171 MHz
Harmonic: <-65dBc below 1 MHz
<-55dBc below 20 MHz
<-45dBc below 80 MHz
<-35dBc below 171 MHz
(channel-channel isolation: <-60dBc)

POWER REQUIREMENTS
+3.14 V to +3.46 VDC@<700 mA, typ: <350 mA.

SIZE
82.6mm by 88.9mm circuit board. Max. height 10mm.

CONNECTORS
MCX for Sine Outputs and EXT CLK IN. 2-pin header for +3.3V power. 24-pin header for high speed control. DE9 for Serial Control. 2-pin wirepoints for LVCMOS.

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Table 2: RS232 Serial Commands

RS232 Command	Function
`Fn xxx.xxxxxxx`	Set Frequency of output “n” in MHz to nearest 0.1 Hz. Decimal point required. n=2, 3. Maximum setting: 171.1276031 MHz. Single tone mode.
`Pn N`	Set Phase of output “n.” N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*π/8192 radians. Sets the relative phase of the frequency output depending upon the value of n=2, 3. Single tone mode.
`E x`	Serial echo control. x=D for Echo **D**isable, x=E for Echo **E**nable
`C x`	Select clock source. x=E for **E**xternal clock, x=I for **I**nternal Clock. May require adjustment of Kp and external filtering of output.
`R`	Reset. This command resets the DDS9m/02. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
`CLR`	Clear. This command clears the EEPROM valid flag and restores all factory default values.
`A x`	x=E for LVCMOS **E**nable, x=D for LVCMOS **D**isable.
`S`	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the `"CLR"` command to return to default values.
`QUE`	Return present frequency, phase and status. Returns a character string of all internal settings.
`M N`	Mode command. Mode ‘0’ is single tone on all channels (default). If N=a, then the phase is automatically cleared during each command ; if N=n, then the phase is not cleared (default). See manual for details.
`Vn N`	Set voltage level of output “n.” In default, the amplitude is set to the maximum: approximately 1V_{pp} (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is digitally scaled by N/1023. n=2, 3 to set the amplitude on frequency 2, 3. If N >=1024, the scaling is turned off and the selected output is set to full scale.
`Vs N`	Set the output scaling factor. N=1 for fullscale, N=2 for half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
`Kp aa`	Set PLL reference multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01_h, 04_h to 14_h). Values of Kp times clock frequency must not be between 160 MHz and 255 MHz (for internal clock, this disallows 5<=Kp<= 9).
`I x`	Set the I/O update pulse method. If x=a, then an I/O update is issued **a**utomatically at the end of each serial command (default). If x=m, then a **m**anual I/O update pulse is expected to be sent by a subsequent `‘I p’` command.
B aa[bb[cc[dd[ee[ff[gg]]]]]]	This **B**yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the function. Please consult the DDS chip data sheet for details. Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed.