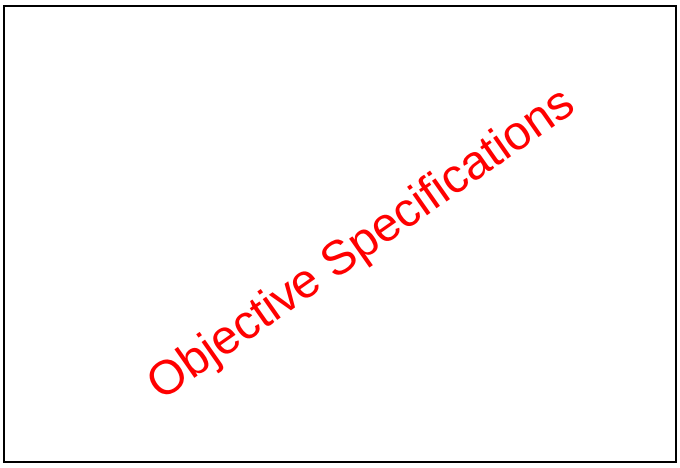
NOVATECH INSTRUMENTS, INC.

Frequency and Phase Agile 150 MHz Signal Generator Module

Model DDS8s



The DDS8s is a 150 MHz Frequency and Phase Agile Synthesized Signal Generator on a modular circuit board. The DDS8s generates Sine, LVCMOS, and LVDS output signals simultaneously up to 150 MHz in 3.333$\overline{3}$ µHz steps under control from a fast differential Synchronous Serial Port (SSP). The SSP allows 48-bits of frequency and 14-bits of phase to be switched in less than 3 µs from a customer supplied controller. Multiple DDS8s can be synchronized and used to generate the fast-switching signals needed for radar, acoustic testing and similar applications. The DDS8s comes with a ±1.5ppm on-board TCXO clock or can be phase locked to an 125 MHz external reference. When locked, the DDS8s has the same accuracy and long term stability as the external reference.

Specifications:

OUTPUTS

TYPES: Sine, LVCMOS and LVDS simultaneously.
IMPEDANCE: 50 Ω.
RANGE: 100 kHz to 150 MHz with 3.333$\overline{3}$ µHz resolution per LSB (10 µHz/3).
SINE AMPLITUDE: approximately +7dBm (0.5 Vrms) into 50 Ω load.
OUTPUT FILTER: Bessel maximally flat delay (MFD) characteristic for optimum phase performance.

LVCMOS AMPLITUDE

V_{OL}<0.5 V, V_{OH}>2.0 V into a series-terminated 15 pF load.
$T_{r,f}$ <2.5 ns. Duty Factor: 45-55%. 50 Ω.

LVDS AMPLITUDE

Meets EIA-644A specifications when terminated into a 100 Ω differential load (TI SN65LVDS100, or equivalent).

CONTROL

Output frequency (48-bits) and phase (14-bits) are controlled by a differential Synchronous Serial Port (SSP). Signal input levels on the SSP meet EIA-644A specifications and have internal differential termination of 100 Ω. (TI SN65LVDT348 or equivalent). Maximum SSP clock rate is 40 MHz. A total of 80 bits is required for the SSP which includes a 16-bit control word.

ACCURACY AND STABILITY

Accuracy: < ±1.5ppm at 10-40 ^{o}C. Stable to an additional ±2ppm per year, 18-28 ^{o}C. (Internal Clock)

EXTERNAL CLOCK IN

LEVEL: 0.25-1.0 Vrms Sine or Square Wave. 50 Ω.
LOCKED: Phase locked to 125 MHz, jumper selectable. (lock range is at least ±25ppm).

SPECTRAL PURITY (Typ. 50 Ω load, internal clock)

Phase Noise: <-120dBc, 10 kHz offset, 10 MHz out.
Spurious: <-70dBc below 10 MHz (300 MHz span)
<-65dBc below 50 MHz
<-50dBc below 150 MHz
Harmonic: <-65dBc below 1 MHz
<-60dBc below 10 MHz
<-50dBc below 25 MHz
<-40dBc below 50 MHz
<-35dBc below 150 MHz

SWITCHING TIME

SSP Control: Frequency and phase switch in approximately 2 µs depending upon customer supplied hardware.

POWER REQUIREMENTS

3.15 to 3.45 VDC@ <750 mA.

SIZE

10.5 cm by 9.1 cm circuit board, excluding connectors. Maximum height 2.5 cm.

CONNECTORS

RA SMAs for SINE Out, LVCMOS Out, LVDS out, EXT CLK In. 2-pin header for Power. 16-pin header for SSP.

1-Jun-2009

NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America
http://www.novatech-instr.com/
sales@novatech-instr.com
206.363.4367 FAX/206.301.8986 Voice