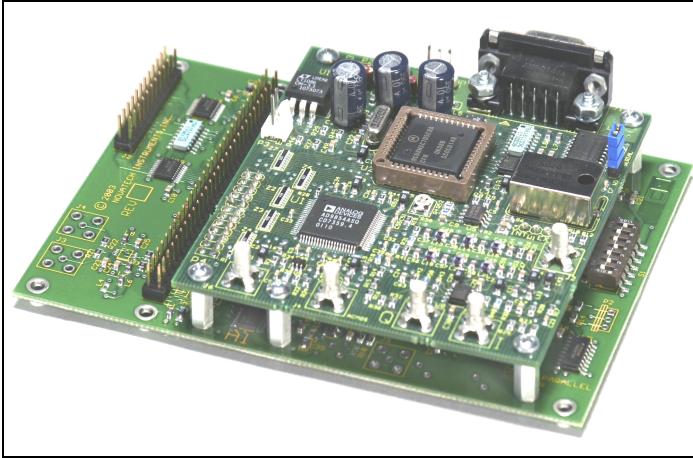


NOVATECH INSTRUMENTS, INC.

Frequency and Phase Agile 120MHz Signal Generator Module Model DDS8p



The DDS8p is a 120MHz Frequency and Phase Agile Synthesized Signal Generator on a modular circuit board. The DDS8p generates Sine, Cosine and AC/MOS/TTL output signals simultaneously up to 120MHz in 1 μ Hz steps under fast parallel binary control. This allows 48-bits of frequency and 14-bits of phase to be switched in approximately 600ns from a customer supplied controller. Multiple DDS8p can be synchronized and used to generate the fast-switching signals needed for radar, acoustic testing and similar applications. For less demanding applications and setup, an RS232 control port is also provided. The DDS8p comes with a \pm 1ppm on-board TCXO clock or it can accept an external clock source up to 300MHz.

Specifications:

OUTPUTS

TYPES: Sine, Cosine and AC/MOS/TTL simultaneously.
IMPEDANCE: 50 Ω .
RANGE: 100Hz to 120MHz in 1 μ Hz steps (int. clock) (2 μ Hz, RS232).
SINE/COS AMPLITUDE: approximately +7dBm (0.5Vrms) into 50 Ω load. Programmable from 0/4096 to 4095/4096 of Full Scale (12-bits control, RS232).
CLOCK OUTPUT: Approximately 1Vpp level clock at the oscillator or external clock frequency. (50 Ω for daisy-chaining multiple units which are to remain phase synchronous.)

AC/MOS/TTL AMPLITUDE

$V_{OL} < 0.5V$, $V_{OH} > 2.5V$ into a series terminated 15pF load.
 $T_{r,f} < 5ns$. Duty Factor: 45-55%. 50 Ω .

CONTROL

Output frequency (48-bits) and phase (14-bits) are controlled either by a fast parallel binary port or an RS232 serial port at 19.2kbaud. RS232 control allows nonvolatile storage of settings. Control method is jumper selectable and detected upon power up. (see the DDS8m datasheet for optimized serial use)

ACCURACY AND STABILITY

Accuracy: $< \pm 1ppm$ at 10-40 $^{\circ}C$. Stable to an additional $\pm 2ppm$ per year, 18-28 $^{\circ}C$. (Internal Clock)

EXTERNAL CLOCK IN

LEVEL: 0.35-2.5Vrms Sine or Square Wave. 50 Ω .
FREQUENCY: 5MHz to 75MHz. Multiplier of 4 to 20

selected via control port (may be bypassed for up to 300MHz direct input). (Output may require additional filtering for optimum performance with external clock.)

SPECTRAL PURITY (Typ. 50 Ω load, internal clock)

Phase Noise: $< -140dBc$, 10kHz offset, 5MHz out.
Spurious: $< -70dBc$ below 10MHz (240MHz span)
 $< -65dBc$ below 40MHz
 $< -50dBc$ below 120MHz
Harmonic: $< -65dBc$ below 1MHz
 $< -60dBc$ below 10MHz
 $< -50dBc$ below 20MHz
 $< -40dBc$ below 50MHz
 $< -35dBc$ below 120MHz

SWITCHING TIME

Parallel Control: Frequency and phase switch in approximately 600ns depending upon customer supplied hardware. RS232 control depends upon host speed and commands sent, typ. $< 10ms$ for a new frequency.

POWER REQUIREMENTS

4.75 to 5.25V @ $< 1.0A$ and -5.25 to -4.75V @ $< 100mA$.

SIZE

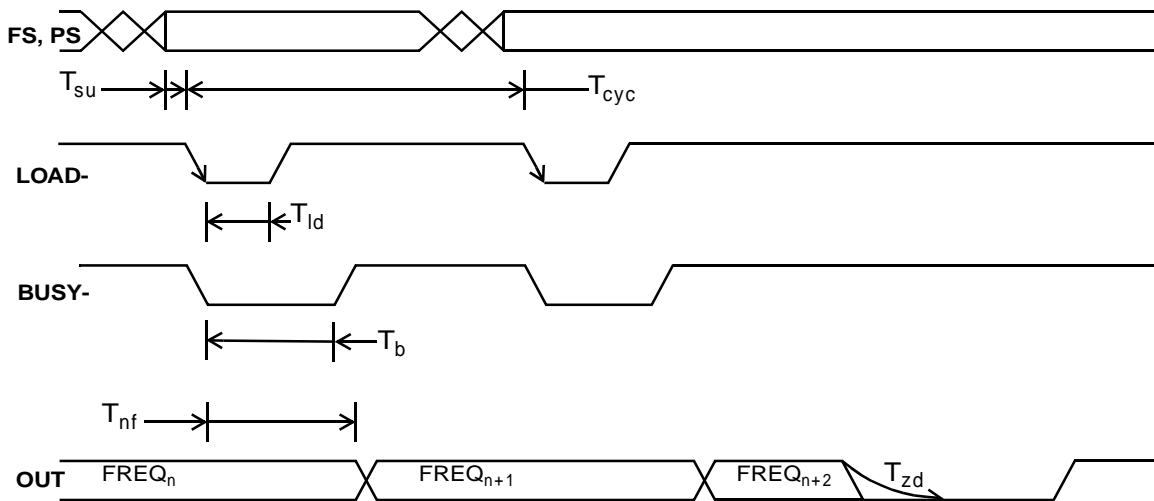
13cm by 9.1cm circuit board, excluding connectors. Maximum height 2.5cm.

CONNECTORS

SMBs for Cosine(I), Sine(Q), AC/MOS/TTL, CLK OUT and EXT CLK IN. 3-pin header for Power. 60pin header for frequency and control, 24pin header for phase.

2-Jul-2003

Parallel Input Timing Diagram (Not to Scale)



Parameter	Name	Min	Max	Notes
T_{su}	Binary Data Setup	10ns		Binary Data Stable before LOAD-.
T_{ld}	Load Pulse Width Low	25ns		Minimum Load pulse width.
T_b	Busy Time		430ns	Busy- is LOW for internal data transfer.
T_{nf}	New Frequency Time		600ns	New frequency on output.
T_{zd}	Zero Decay Time		100 μ s TYP	Time for Output to decay to ± 100 mV (for zero frequency setting).
T_{cyc}	Load cycle time	600ns		Cycle time before next LOAD- time.

P1 Pin Number	Function	P1 Pin Number	Function
1	Frequency Select 1 (FS1)	2	Frequency Select 0 (FS0) (LSB)
3	FS3	4	FS2
[...]	[...]	[...]	[...]
47	FS47 (MSB)	48	FS46
49	Circuit Common (GROUND)	50	BUSY- (OUTPUT)
51	LOAD-	52	Circuit Common (GROUND)
53	nc	54	IOUDm- (leave open)
55	nc	56	nc
57	RES- (must be OPEN on REV-assemblies)	58	nc
59	Circuit Common (GROUND)	60	Circuit Common (GROUND)

Frequency connector shown. Phase connector is similar, but only 24-pins total.