MODEL DDS8par 48-bit Binary Parallel Controlled Synthesizer

NOTE:

This is a manual addendum to the Novatech Instruments, Inc. Model DDS8m. This addendum covers the changes made for Model DDS8par which has a high-speed 48-bit parallel binary interface replacing the serial interface of the standard model. The DDS8m manual is included by reference. Please refer to it for details on basic operation and installation.

Specification Changes:

OUTPUT: The output frequency range is 10kHz to 100MHz (Sine, Cosine and ACMOS) in 1μHz steps per LSB on the parallel interface (internal clock).

FREQUENCY CONTROL: The Parallel interface is on a 60-pin (30x2) header (see below for pinout and timing). The RS232 port on the DDS8m board is inoperative on the DDS8par and must remain unconnected.

SIZE: 4.1 inches by 3.6 inches by 1.0 inch high (104.1mm by 91.4mm by 25.4), not including connectors.

CONNECTOR: 30x2 header with 0.025inch square posts on 0.1inch spacing.

DIP SWITCH: A Dip Switch has been added to set Kp (see DDS8m manual for description of Kp).

Installation Notes:

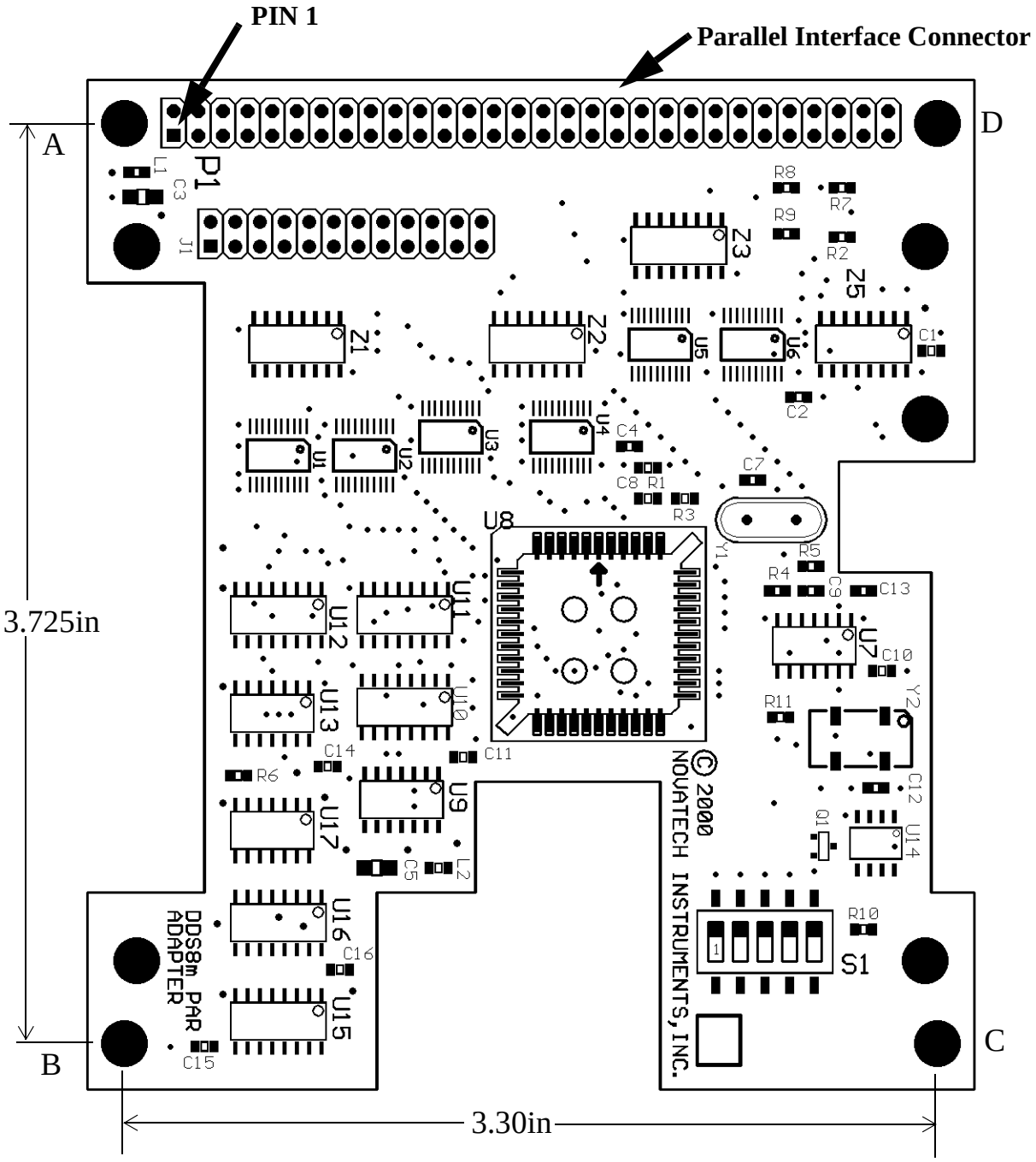
The installation of the DDS8par is similar to the Model DDS8m with the exception of the parallel interface connections. Please refer to the DDS8m manual for basic installation notes.

NOTE:

Use extreme care during installation and removal of 60-pin cabling to the DDS8par. Do not unduly flex the board.

See signal description, timing diagram, timing table and signal notes below for operation of the parallel adapter.

DDS8par Parallel Adapter Component/Connection Location Diagram (Not to Scale)



Holes A, B, C and D are 0.125inch diameter clearance holes. The DDS8par is shipped with 0.75inch, 4-40 Threaded Aluminum Spacers mounted in these holes to allow mounting to a base-plate with clearance for the protruding leads of the DDS8m main board. These holes are electrically connected to circuit common (ground). The unmarked large holes mount the parallel adapter board to the DDS8m. These must be left undisturbed.

Table 1: Parallel Connector Pin Out

Pin Number	Function	Pin Number	Function
1	Frequency Select 1 (FS1)	2	Frequency Select 0 (FS0) (LSB)
3	FS3	4	FS2
5	FS5	6	FS4
7	FS7	8	FS6
9	FS9	10	FS8
11	FS11	12	FS10
13	FS13	14	FS12
15	FS15	16	FS14
17	FS17	18	FS16
19	FS19	20	FS18
21	FS21	22	FS20
23	FS23	24	FS22
25	FS25	26	FS24
27	FS27	28	FS26
29	FS29	30	FS28
31	FS31	32	FS30
33	FS33	34	FS32
35	FS35	36	FS34
37	FS37	38	FS36
39	FS39	40	FS38
41	FS41	42	FS40
43	FS43	44	FS42
45	FS45	46	FS44
47	FS47 (MSB)	48	FS46
49	Factory Only (Tied LOW)	50	BUSY- **(OUTPUT)**
51	LOAD-	52	PULSE- (LOW for Frequency Out)
53	nc	54	nc
55	nc	56	nc
57	RES-	58	nc
59	Circuit Common (GROUND)	60	Circuit Common (GROUND)

Parallel Input Requirements

NOTE:

The parallel inputs do not have additional protection against ESD damage beyond that provided by the CMOS inputs (±2kV, Human Body Model. ±200 V, machine model).

The inputs on the DDS8par are 3.3v and 5.0v CMOS logic tolerant. The BUSY- output is 3.3v VHCMOS logic.

All of the inputs, **FS0-47, LOAD-** and **PULSE-**, are VHCMOS compatible and require:

V_{il} <= 0.3*V_{cc} (nominally 1.0 volts)
V_{ih} >= 0.7*V_{cc} (nominally 2.3 volts)

C_{in} on each pin is approximately 10pF (application cable capacitance not included). All the input pins are pulled to V_{cc} (nominally 3.3v) via pull-up resistors. It is recommended that a series termination resistor of 50-100Ω be used in each signal line to prevent reflections and ringing. The exact value will be determined by your application.

Signal Descriptions:

FS0 through **FS47** are the 48 binary data bits presented to the internal DDS. The frequency output for the default values of Kp and the internal clock will have 1μHz of resolution per LSB. Since there is no error checking of the user's input, care must be taken ensure that the binary value does not select a frequency output greater than approximately 120MHz.

BUSY- is a VHCMOS compatible ***output*** with:

V_{oh} >= 3.0 V (I_{load} <= -100μA)
V_{ol} <= 0.2V (I_{load} <= 100μA)

BUSY- going HIGH indicates that all parallel data has been loaded into the DDS circuitry and the new frequency is stable. The output frequency is updated approximately 10μs *before* BUSY- returns HIGH. Please refer to timing diagram for details.

BUSY- has a series resistance of approximately 500Ω to prevent damage due to accidental shorts. If this output is used for handshaking be sure to account for capacitive loading on this signal.

Please refer to the timing diagram and table below for the details of setting frequency on the parallel interface.

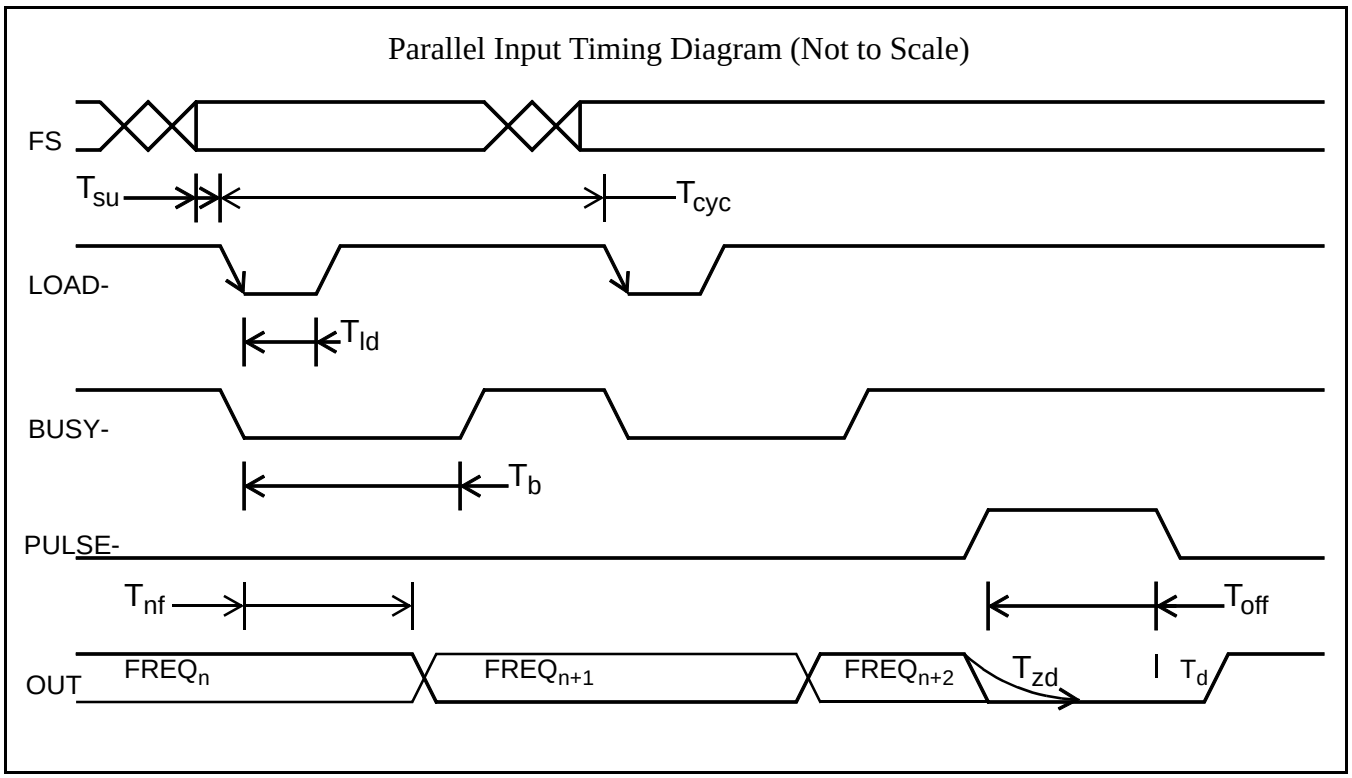


Table 2: Timing, Internal Clock, default Kp.

Parameter	Name	Min	Max	Notes
T_{su}	Binary Data Setup	10ns		Binary Data Stable before LOAD-.
T_{ld}	Load Pulse Width Low	25ns		Minimum Load pulse width.
T_b	Busy Time		100µs	Busy- is LOW for internal data transfer.
T_{nf}	New Frequency Time		90µs	New frequency on output.
T_{off}	Pulse Off Time	1µs		PULSE- must be LOW for output.
T_{zd}	Zero Decay Time		10µs TYP	Time for Output to decay to ±100mV.
T_d	Pulse LOW to output		170ns	Time for output to start after PULSE- goes true (LOW).
T_{cyc}	Load cycle time	125µs TYP		Cycle time before next LOAD- time.

LOAD- going LOW is used to signal the on-board circuitry to load a new frequency into the DDS registers. The negative edge of LOAD- is latched and presented on the BUSY- line. The negative edge also transfers data from the user application connection to internal latches. Data must be stable at least 10ns before the negative edge of LOAD-. During BUSY-, all appropriate registers on the DDS8m are programmed and upon completion of the loading process a new frequency is available at the output. The on-board circuitry takes approximately 10µs to clear the BUSY-

(return it HIGH) after a new frequency is stable. The timing of BUSY- returning HIGH may have several microseconds of ambiguity due to timing re-synchronization internal to the parallel interface board.

PULSE-, which must be LOW to obtain a frequency output, can be used to generate a pulsed output frequency which begins with zero phase. The *positive* edge of PULSE- initiates a sequence which turns off the output frequency and then zeroes its phase, which takes approximately 1μs. Due to AC-coupling time constants, the decay to zero volts takes another 10μs. Customer supplied circuitry may reduce this by terminating the pulse on a known output phase. PULSE- going LOW initiates the output frequency at the last value loaded by the LOAD- signal. PULSE- LOW to valid frequency output takes approximately 170ns.

PULSE- can be used to synchronize the output of a new frequency. If PULSE- is kept HIGH during a LOAD- pulse and subsequent BUSY- period, returning it LOW will initiate a new frequency. Note, however, that the phase is not controlled in this mode. Phase reset to zero must be initiated by a positive edge on PULSE-.

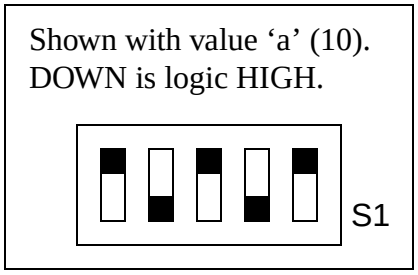
NOTE:

The ACMOS output may be erratic in Pulse mode due to internal time constants. If an ACMOS signal is required in pulse applications, it is recommended that the customer consider external level shifting circuitry. Best pulse performance is obtained from the 'Q' Channel.

RES- is the reset signal. When LOW all the circuitry on the DDS8m and the DDS8m parallel adapter is reset. Upon returning HIGH, the DDS8par will initialize in less than 250ms and output a frequency of 10MHz (internal clock and default Kp).

Note that pin 49 is for factory test only and is tied LOW on board the DDS8par.

Setting Kp. The internal clock multiplier is set by Dip Switch, S1, and is a default value of 10 (hexadecimal 'a'). Valid settings are the same as the DDS8m: 1 and 4 to 20. S1 is set in binary. See the figure below.



After a power cycle, the DDS8par takes approximately 250msec to initialize.

WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

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All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, Washington 98155-0997
United States of America

FAX: 206.363.4367
TEL: 206.301.8986
http://www.novatech-instr.com/
novatech@eskimo.com