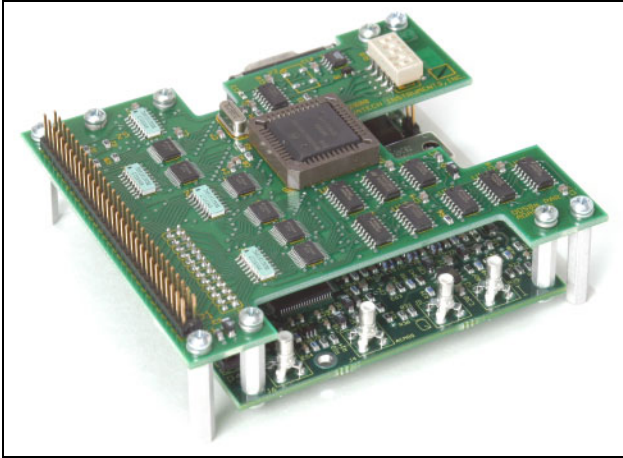


NOVATECH INSTRUMENTS, INC.

Frequency Agile 100MHz Signal Generator Module Model DDS8par



The DDS8par is a 100MHz Frequency Agile Synthesized Signal Generator on a modular circuit board. The DDS8par generates Sine, Cosine and AC/MOS/TTL output signals simultaneously up to 100MHz in 1 μ Hz steps under parallel binary control. This allows 48-bits of frequency to be switched in approximately 100 μ s from a customer supplied controller. Multiple DDS8par can be synchronized and used to generate the fast-switching signals needed for radar, acoustic testing and similar applications. The DDS8par comes with a \pm 1.5ppm on-board TCXO clock or it can accept an external clock source up to 300MHz.

Specifications:

OUTPUTS

TYPES: Sine, Cosine and AC/MOS/TTL simultaneously.
IMPEDANCE: 50 Ω .

RANGE: 100Hz to 100MHz in 1 μ Hz steps (int. clock).

SINE/COS AMPLITUDE: approximately +7dBm
(0.5V_{rms}) into 50 Ω load.

CLOCK OUTPUT: Approximately 1V_{pp} level clock at the oscillator or external clock frequency. (50 Ω for daisy-chaining multiple units which are to remain phase synchronous.)

AC/MOS/TTL AMPLITUDE

V_{OL}<0.5V, V_{OH}>2.5V into a series terminated 15pF load.

T_{r,f}<5ns. Duty Factor: 45-55%. 50 Ω .

CONTROL

Output frequency is controlled by a 48-bit parallel binary port. Frequency switches in <100 μ s depending upon customer supplied hardware. See timing diagram and connector pin-out on next page.

ACCURACY AND STABILITY

Accuracy: < \pm 1.5ppm at 10-40 $^{\circ}$ C. Stable to an additional \pm 2ppm per year, 18-28 $^{\circ}$ C. (Internal Clock)

EXTERNAL CLOCK IN

LEVEL: 0.35-2.5V_{rms} Sine or Square Wave. 50 Ω .

FREQUENCY: 5MHz to 75MHz. Multiplier of 4 to 20 selected via on-board switch. (Output may require additional filtering for optimum performance with external clock.) Multiplier can be bypassed for up to 300MHz input.

SPECTRAL PURITY (Typ. 50 Ω load, internal clock)

Phase Noise: <-140dBc, 10kHz offset, 5MHz out.

Spurious: <-70dBc below 10MHz (200MHz span)

<-65dBc below 40MHz

<-50dBc below 100MHz

Harmonic: <-65dBc below 1MHz

<-60dBc below 10MHz

<-50dBc below 20MHz

<-40dBc below 50MHz

<-35dBc below 100MHz

POWER REQUIREMENTS

4.75 to 5.25V@ <0.9A and -5.25 to -4.75V@ <100mA.

SIZE

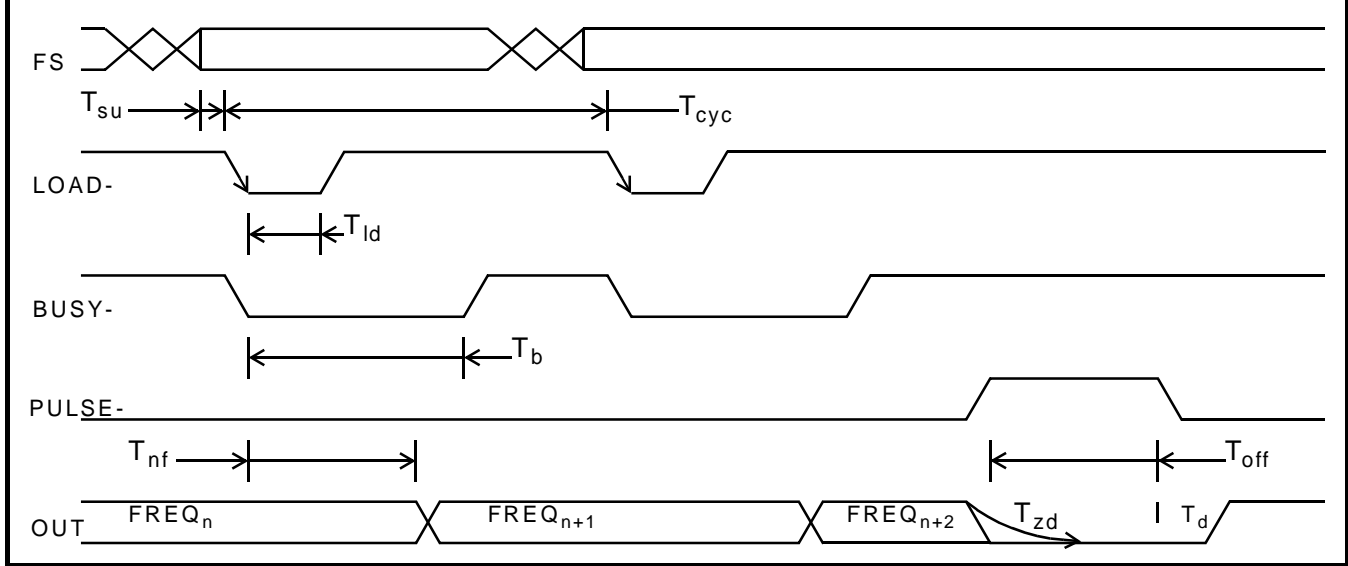
10.4cm by 9.1cm circuit board, excluding connectors.
Maximum height 2.5cm.

CONNECTORS

SMBs for Cosine(I), Sine(Q), AC/MOS/TTL, CLK OUT and EXT CLK IN. 3-pin header for Power. 60pin header for frequency and control.

23-Jan-2006

Parallel Input Timing Diagram (Not to Scale)



Parameter	Name	Min	Max	Notes
T_{su}	Binary Data Setup	10ns		Binary Data Stable before LOAD-.
T_{ld}	Load Pulse Width Low	25ns		Minimum Load pulse width.
T_b	Busy Time		100 μ s	Busy- is low for internal data transfer.
T_{nf}	New Frequency Time		90 μ s	New frequency on output.
T_{off}	Pulse Off Time	1 μ s		PULSE- must be low for output.
T_{zd}	Zero Decay Time		10 μ s TYP	Time for Output to decay to ± 100 mV.
T_d	Pulse low to output		170ns	Time for output to start after PULSE- goes true (LOW).
T_{cyc}	Load cycle time	125 μ s TYP		Cycle time before next LOAD- time.

P1 Pin Number	Function	P1 Pin Number	Function
1	Frequency Select 1 (FS1)	2	Frequency Select 0 (FS0) (LSB)
3	FS3	4	FS2
[...]	[...]	[...]	[...]
47	FS47 (MSB)	48	FS46
49	Factory Only (Tie LOW)	50	BUSY- (OUTPUT)
51	LOAD-	52	PULSE- (LOW for Frequency Out)
53	nc	54	nc
55	nc	56	nc
57	RES-	58	nc
59	Circuit Common (GROUND)	60	Circuit Common (GROUND)