NOVATECH
INSTRUMENTS, INC.

Model DDS8p 48-bit Frequency Agile 120MHz Synthesizer

NOTE:

This is a manual addendum to the Novatech Instruments, Inc. Model DDS8m covering the changes made for Model DDS8p, which has high-speed 48-bit parallel binary frequency and 15-bit parallel binary phase interfaces in addition to the serial interface of the standard model. The DDS8m manual is included by reference; please refer to it for details on basic operation and installation.

Specifications (in addition to DDS8m):

OUTPUT: The output frequency range is 100Hz to 120MHz (Sine, Cosine and ACMOS) in 1μHz steps per LSB on the parallel interface (internal clock and default settings).

PARALLEL CONTROL: The Parallel interface is on a 60-pin header for frequency (backwards compatible with the DDS8m/03 and PAR-48) and on a 24-pin header for phase control (see below for pinout and timing). The RS232 port on the DDS8p board can be enabled by setting W3, see details below. (Only Mode 0 can be used during serial operation.)

SIZE: 5.1 inches by 3.6 inches by 1.0 inch high (129.5mm by 91.4mm by 25.4mm), not including connectors.

CONNECTORS: 30x2 header with 0.025inch (0.635mm) square posts on 0.1inch (2.54mm) spacing for Frequency; 12x2 for Phase. A 3-pin header is provided for power (same as DDS8m).

Installation Notes:

The installation of the DDS8p is similar to the Model DDS8m with the exception of the parallel interface connections. Please refer to the DDS8m manual for basic installation notes.

The default initialization values (the output after a power-up but before a LOAD- pulse has been issued) can be set by putting the DDS8p into RS232 serial mode. This is accomplished by installing W3, cycling power and using the serial commands detailed in the DDS8m manual. Once the desired settings are established, use the `'SAVE'` command to store the values. Remove W3 and again cycle power. The DDS8p will then initialize with the values set by the `'SAVE'` command. Please note that the DDS8p implements only **Mode 0** of the DDS8m. Parallel operation and serial operation are mutually exclusive. In serial mode, the timing of the standard

DDS8m module applies.

The on-board dip switch (S1, see component placement diagram) is used for factory test, except for the EXT/INT Select position. When pushed toward the board edge, the internal VCTCXO is selected. When set away from the board edge, the external clock is used. The internal source is always used for internal timing on the DDS8p board. Default setting is for the internal clock.

WARNING:

Use extreme care during installation and removal of cabling to the DDS8p. Do not unduly flex the board, which could result in damaged surface-mounted components.

See signal description, timing diagram, timing table and signal notes below for operation of the parallel adapter connectors.

Parallel Input Requirements

NOTE:

The parallel inputs do not have additional protection against ESD damage beyond that provided by the CMOS inputs (±2kV, Human Body Model. ±200 V, machine model).

The inputs on the DDS8p are 3.3v and 5.0v CMOS logic tolerant. The BUSY- output is 3.3v VHCMOS logic.

All of the inputs, **FS0-47, LOAD-** and **IOUDm-**, are VHCMOS compatible and require:

V_{il} <= 0.3*V_{cc} (0.9 volts max) (1.0 volts nominal)
V_{ih} >= 0.7*V_{cc} (2.5 volts min) (2.3 volts nominal)

NOTE:

Using TTL input signals may not provide acceptable noise margins, depending upon your application circuitry; 3.3V VHCMOS logic levels are suggested.

C_{in} on each pin is approximately 10pF (application cable capacitance not included). All the input pins are pulled to V_{cc} (nominally 3.3v) via pull-up resistors. It is recommended that a series termination resistor of 50-100Ω be used in each signal line to prevent reflections and ringing. The exact value will be determined by your application.

Signal Descriptions:

FS0 through **FS47** are the 48 binary data bits presented to the internal DDS frequency output register. The frequency output for the default values of Kp and the internal clock will have 1µHz of resolution per LSB. Since there is no error checking of the user input, care must be taken to

ensure that the binary value does not select a frequency output greater than approximately 120MHz to maintain acceptable filtering performance.

PS0 through **PS13** are the 14 binary data bits presented to the internal DDS phase offset register. Note that the Sine and Cosine outputs are always a nominal 90^o apart. This phase setting offsets the DDS8p from an arbitrary reference (see IOUDm- below). The phase offset is $N*360^o/16384$ or $N*\pi/8192$, were N is the binary value of PS0 through PS13 (maximum value 16,383).

BUSY- is a VHCMOS compatible ***output*** with:

V_{oh} >= 3.0 V (I_{load} <= -100µA)
V_{ol} <= 0.2V (I_{load} <= 100µA)

BUSY- going HIGH indicates that all parallel data has been loaded into the DDS circuitry and the new frequency will become stable approximately 170ns later. Please refer to timing diagram for details.

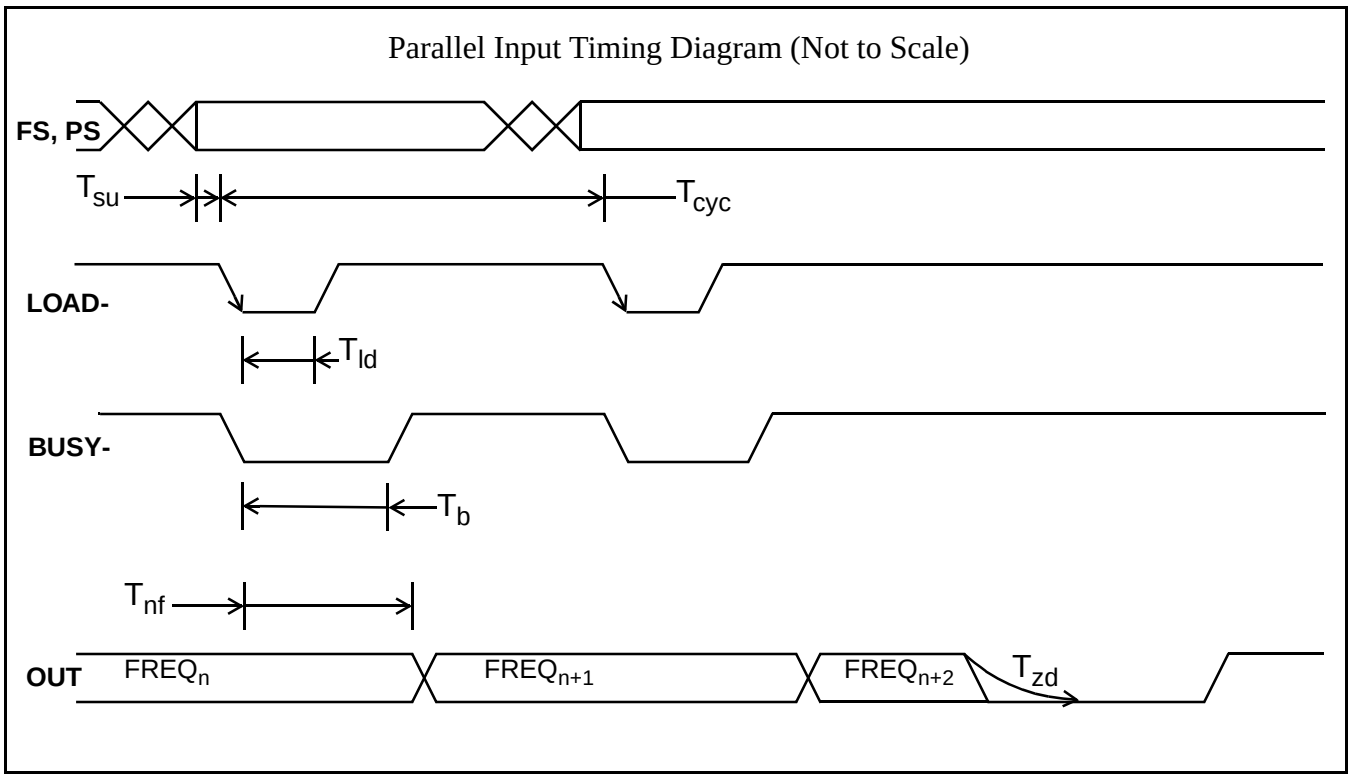
BUSY- has a series resistance of approximately 500Ω to prevent damage due to accidental shorts. If this output is used for handshaking, be sure to account for capacitive loading on this signal.

Please refer to the timing diagram and table below for the details of setting frequency and phase on the parallel interface.

Table 1: Timing, Internal Clock, default Kp.

Parameter	Name	Min	Max	Notes
T_{su}	Binary Data Setup	10ns		Binary Data Stable before LOAD-.
T_{ld}	Load Pulse Width Low	25ns		Minimum Load pulse width.
T_b	Busy Time		430ns	Busy- is LOW for internal data transfer.
T_{nf}	New Frequency Time		600ns	New frequency on output.
T_{zd}	Zero Decay Time		100µs TYP	Time for Output to decay to ±100mV (for zero frequency setting).
T_{cyc}	Load cycle time	600ns		Cycle time before next LOAD- time.

LOAD- going LOW is used to signal the on-board circuitry to load a new frequency into the DDS registers. The negative edge of LOAD- is latched and presented on the BUSY- line. The negative edge also transfers data from the user application connection to internal latches. Data must be stable at least 10ns before the negative edge of LOAD-. During BUSY-, all appropriate registers on the DDS8m are programmed and, upon completion of the loading process (BUSY- returning HIGH), a new frequency is available at the output after approximately 170ns of pipeline delay. The timing of BUSY- returning HIGH may have up to ±36ns of ambiguity due to timing synchronization internal to the parallel interface board.



NOTE:

The ACMOS output may be erratic when pulsing the output due to internal time constants (T_{zd}). If an ACMOS signal is required in pulse applications, it is recommended that the customer consider external level shifting circuitry. Best pulse performance is obtained from the 'Q' Channel.

RES- is the reset signal. When LOW all the circuitry on the DDS8m and the DDS8m parallel adapter is reset. Upon returning HIGH, the DDS8p will initialize in approximately 1sec and output a frequency of 10MHz (internal clock and default Kp). ***(This signal is not implemented on Rev- assemblies. A power cycle is required for reset).***

IOUDm- is a "master" I/O update signal. This signal can be used to synchronize multiple DDS8p. Normally left open (pulled HIGH on board), IOUDm- can be held LOW during a frequency/phase LOAD- and BUSY- time. Upon release to OPEN or HIGH, all DDS8p connected to the same line will transfer the loaded data into the active registers on the DDS ASIC. This will start each DDS8p board output at the same time. If used with a common external clock, all of the common connected DDS8p will then remain phase synchronous.

Table 2: P1, Frequency Data and Control Connector.

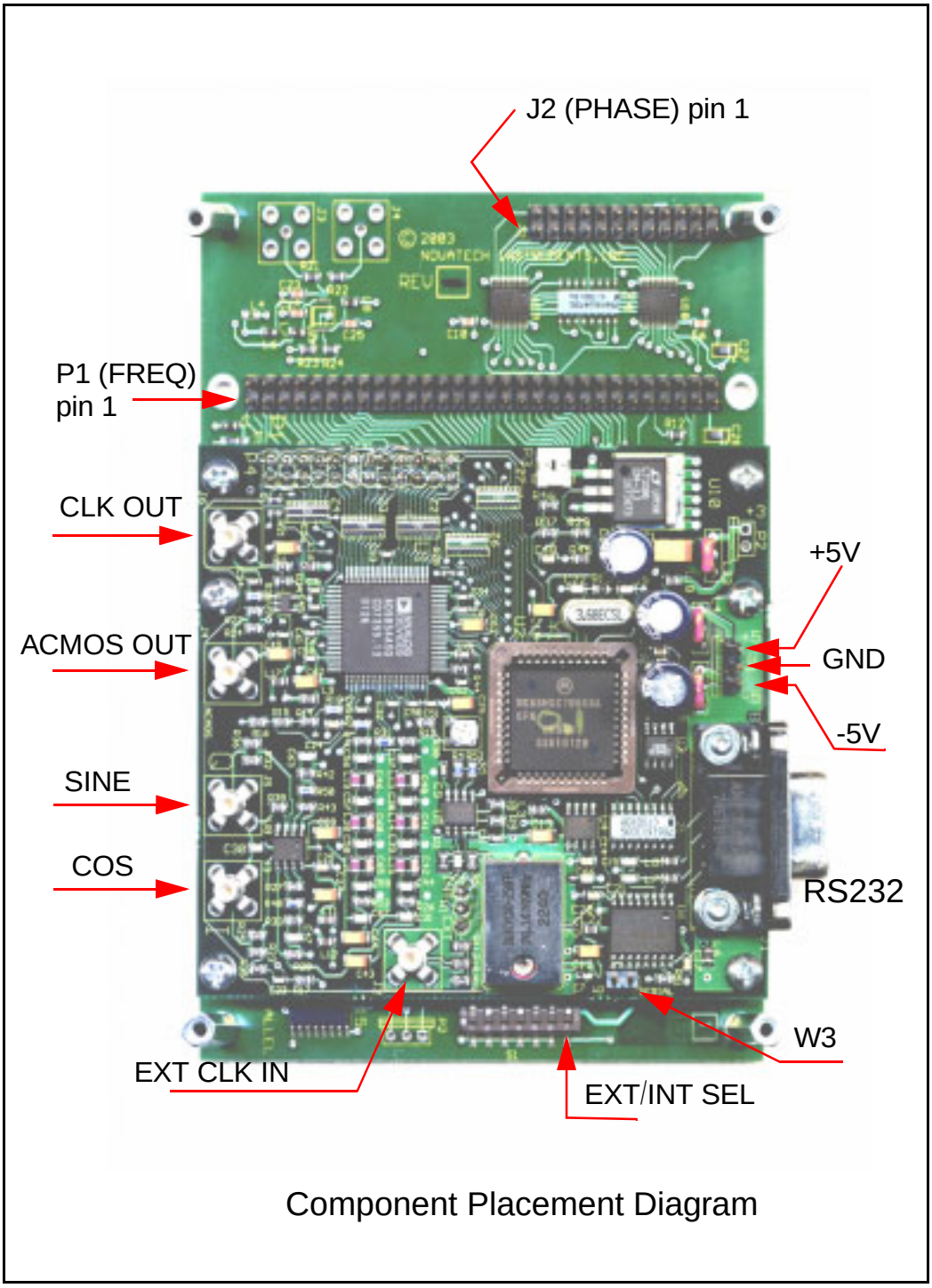
P1 Pin Number	Function	P1 Pin Number	Function
1	Frequency Select 1 (FS1)	2	Frequency Select 0 (FS0) (LSB)
3	FS3	4	FS2
5	FS5	6	FS4
7	FS7	8	FS6
9	FS9	10	FS8
11	FS11	12	FS10
13	FS13	14	FS12
15	FS15	16	FS14
17	FS17	18	FS16
19	FS19	20	FS18
21	FS21	22	FS20
23	FS23	24	FS22
25	FS25	26	FS24
27	FS27	28	FS26
29	FS29	30	FS28
31	FS31	32	FS30
33	FS33	34	FS32
35	FS35	36	FS34
37	FS37	38	FS36
39	FS39	40	FS38
41	FS41	42	FS40
43	FS43	44	FS42
45	FS45	46	FS44
47	FS47 (MSB)	48	FS46
49	Circuit Common (GROUND)	50	BUSY- ***(OUTPUT)***

Table 2: P1, Frequency Data and Control Connector.

P1 Pin Number	Function	P1 Pin Number	Function
51	LOAD-	52	Circuit Common (GROUND)
53	nc	54	IOUDm- (leave open)
55	nc	56	nc
57	RES- (must be OPEN on REV- assemblies)	58	nc
59	Circuit Common (GROUND)	60	Circuit Common (GROUND)

Table 3: J2, Phase Data.

J2 Pin Number	Function	J2 Pin Number	Function
1	Phase Select 1 (PS1)	2	Phase Select 0 (PS0) (LSB)
3	PS3	4	PS2
5	PS5	6	PS4
7	PS7	8	PS6
9	PS9	10	PS8
11	PS11	12	PS10
13	PS13 (MSB)	14	PS12
15	nc	16	***Do Not Connect***
17	nc	18	nc
19	nc	20	nc
21	nc	22	nc
23	Circuit Common (GROUND)	24	Circuit Common (GROUND)



Component Placement Diagram

Hardware Mounting: The DDS8m synthesizer module is attached to the DDS8p parallel adapter board using 6 aluminum spacers and 12 screws. These must remain undisturbed. There are 6 free mountings holes with clearance for 3mm or #4 screws. The mounting hole pad is connected to Circuit Common (ground). It is suggested that all 6 positions be used to attach board into the application. Please leave approximately 3mm clearance spacing from the bottom of the board.

WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

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