Instruments, Inc.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America

DDS8m/06 Addendum to DDS8m Synthesizer Module Manual

The Model DDS8m/06 is a firmware-modified version of the Model DDS8m 100MHz Quadrature Synthesizer Module to allow external hardware to generate a "pulsed-chirp" frequency. All parameters are entered via the serial port, while the pulse duration and timing are controlled by external customer supplied hardware (an example set of hardware is shown below).

Use the DDS8m Instruction Manual for installation and operating instructions.

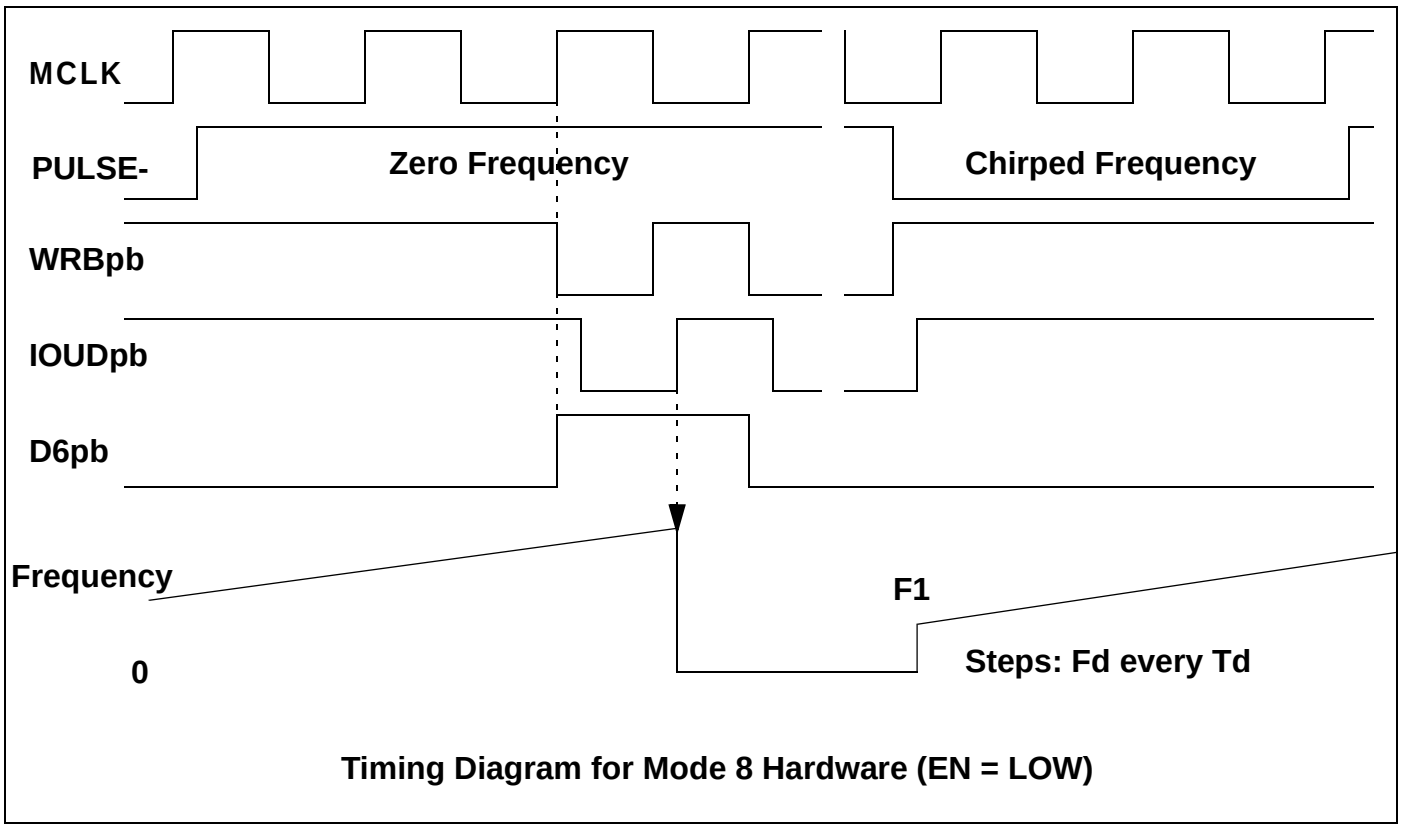
A new mode command (Table 2) is added:

```
M 8
```

The coupling capacitors on the on-board filter have been reduced to give approximately 5µs time constant. Note that elliptic filters are used. Optimum pulse response would require Bessel or similar filter. Please consult Novatech Instruments, Inc. for applications assistance if the pulse response is unacceptable.

This new mode is similar to "M 3" except that external hardware must be used to generate a "pulsed-Chirp" Frequency. In this mode, the external hardware resets the frequency after a period timed by the hardware. In the example hardware shown below, the negative edge of the signal PULSE- restarts a frequency at F1, ramps with a delta-Frequency step of Fd at rate Td. The final frequency is determined by the width of the PULSE- signal. Upon the positive edge of PULSE-, the output frequency is set to zero. See the timing diagram shown below.

Four control signals are required to be connected to the DDS8m parallel connector (P4). These signals are: D6pb, WRBpb, IOUDpb and EN. EN is an output to the customer supplied hardware and is LOW when the hardware is enabled. It goes HIGH when any commands are executed by the DDS8m and returns LOW to re-enable the hardware after an "M 8" command is executed. See the timing diagram for the relationship among the various signals. Note that all signals are 3.3V logic levels-- VHC CMOS is suggested.



Timing Diagram for Mode 8 Hardware (EN = LOW)

Signal Definitions:

MCLK: Master clock supplied by customer. The Clock Output (J6) from the DDS8m can be used (with appropriate level shifting) or any other clock up to approximately 30MHz. Lower frequencies will provide lower noise level.

PULSE-: When low, a chirped frequency will be enabled. With the hardware shown, and PULSE- asynchronous to MCLK, up to three MCLK periods will be required to clear the frequency to zero.

WRBpb, IOUDpb and **D6pb** are derived signals which generate a reset to zero frequency internal to the on-board DDS chip. Any hardware which clocks in a logic 1 on D6pb and then a logic 0 on the positive edges of WRBpb and IOUDpb will perform the required function. IOUDpd is shown slightly delayed from WRBpb, but this can be zero ns. Minimum pulse width on WRBpb, IOUDpb and D6pd is approximately 25ns.

EN: This signal "tri-states" the signals from the external hardware, so that the on-board microcontroller can write to the DDS chip. It is low when the external hardware is enable. It returns high upon any serial communications with the DDS8m and is set low upon execution of an `"M 8"` command.

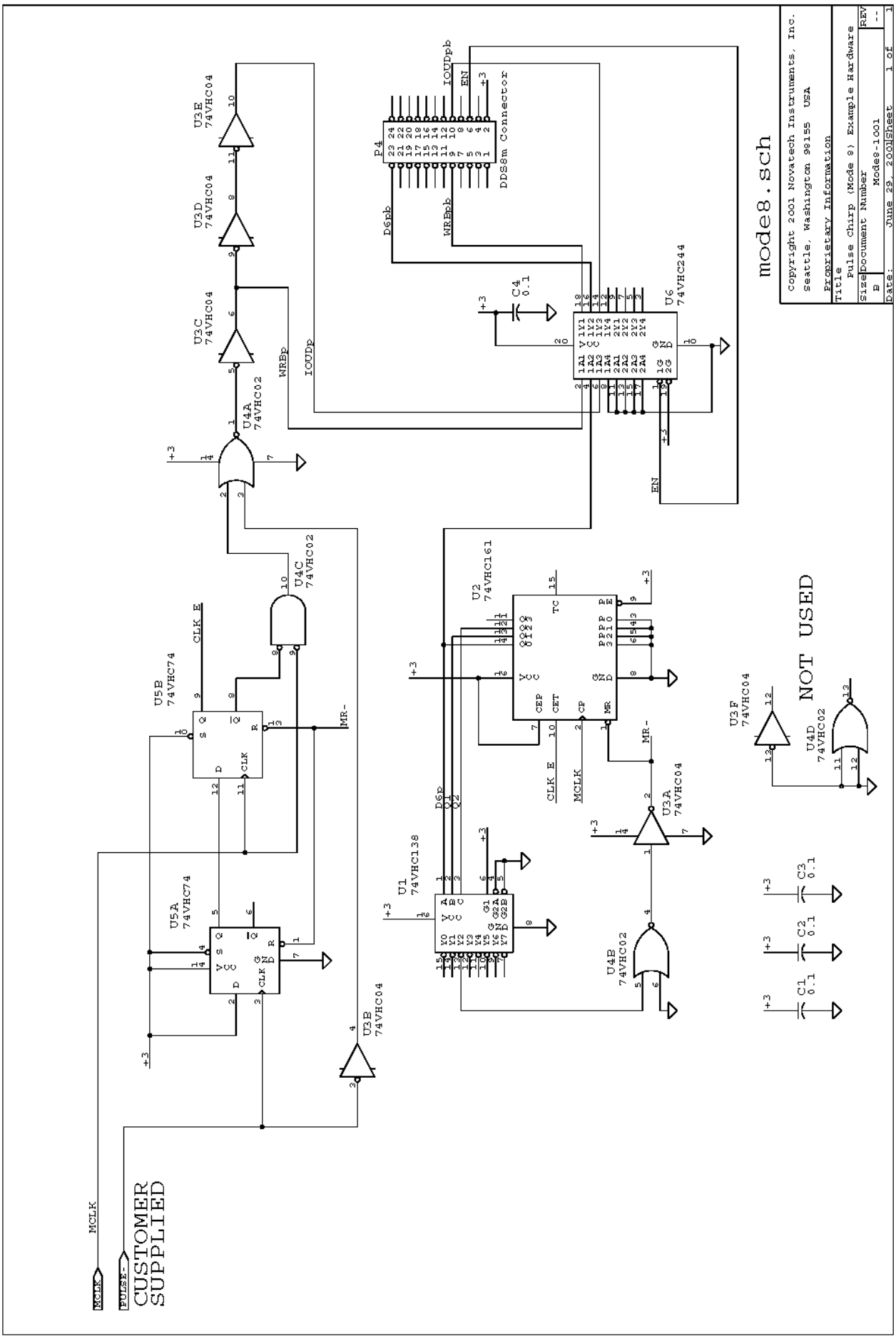
The commands sent to the DDS8m would then be:

```
M 0
F1 16.66
Fd 0.000007910718
Td 1
M 8
```

This assumes the same example as used for Mode 3 in the DDS8m manual. Note that Tr is unused, since the end of the chirp is set by the external hardware.

Note 1: the DC value left on the filter is determined by the phase of the output signal at the termination of the FSK pulse. When the frequency is reset to zero by the hardware, a step of amplitude proportional to the DC value will occur.

Note 2: Pin 8 of P4 must be held low for the Chirp mode to function (also true for Mode 3).


mode8.sch
Copyright 2001 Novatech Instruments, Inc.
Seattle, Washington 98155 USA
Proprietary Information
Title
Pulse Chirp (Mode 8) Example Hardware
Size
B
Document Number
Mode8-1001
REV
--
Date: June 29, 2001
Sheet 1 of 1
CUSTOMER SUPPLIED
MCLK
PULSE-
NOT USED
U1 74VHC138
U2 74VHC161
U3A 74VHC04
U3B 74VHC04
U3C 74VHC04
U3D 74VHC04
U3E 74VHC04
U3F 74VHC04
U4A 74VHC02
U4B 74VHC02
U4C 74VHC02
U4D 74VHC02
U5A 74VHC74
U5B 74VHC74
U6 74VHC244
P4
DDS8m Connector
C1 0.1
C2 0.1
C3 0.1
C4 0.1
+3
MR-
CLK E
MCLK
WRBp
IOUDp
IOUDpb
WRBpb
D6pb
D6p
EN