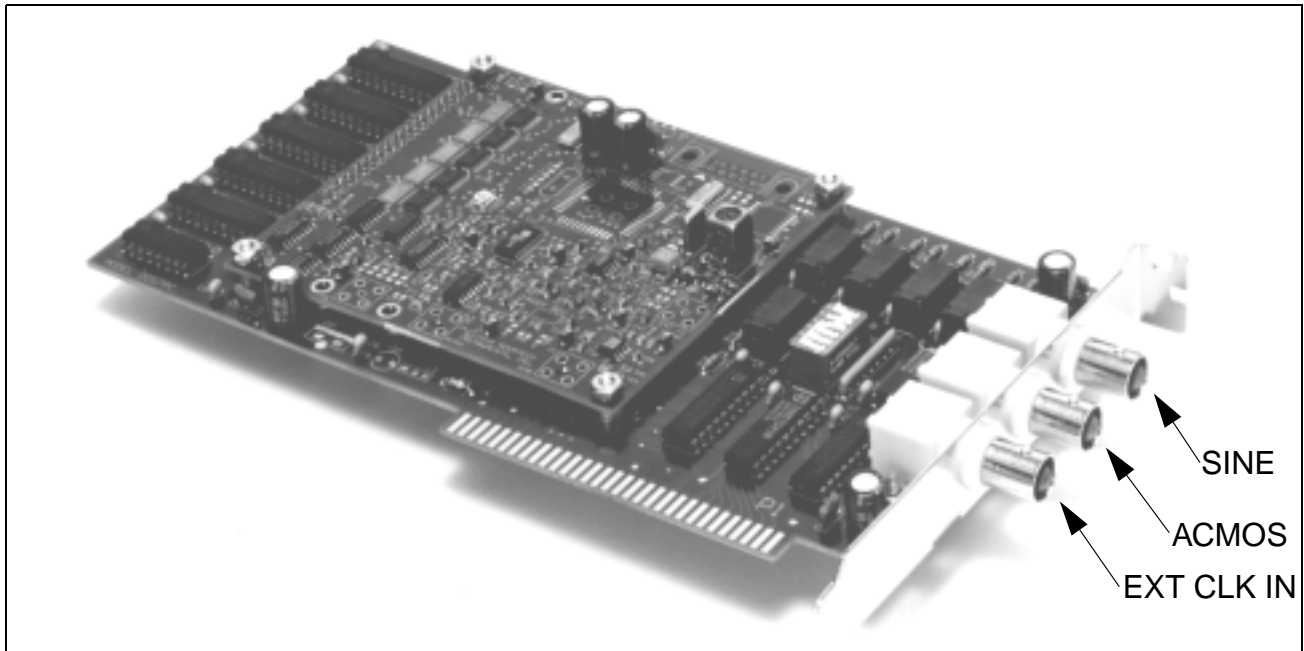


NOVATECH INSTRUMENTS, INC.

INSTRUCTION MANUAL Model DDS7pc 68MHz DDS Signal Generator



DDS7pc

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1.0 DESCRIPTION

1.1 The Model DDS7pc is a 68MHz Direct Digital Synthesizer on a printed wiring board for installation in a PC, XT or PC AT or later ISA-bus computer, using only an 8-bit slot. The DDS7pc provides both Sine and AC MOS output signals, which can be set from 100Hz to 68MHz in 0.04Hz steps when using the internal clock.

1.2 The DDS7pc can also be used with an External Clock input. An on-board x6 frequency multiplier generates the master clock allowing user configured frequency ranges. When used with an external clock, multiple DDS7pc are phase synchronous. When using an external clock, customer supplied filters may be required for optimum performance.

1.3 The DDS7pc is supplied with Source and Compiled application software. This software is written in 'C' and is compatible with the GNU C-compiler.

2.0 SPECIFICATIONS

2.1 OUTPUTS

TYPES: Sine and AC MOS/TTL Simultaneously.

IMPEDANCE: 50 Ω .

FREQUENCY: 100Hz to 68MHz in 0.04Hz steps, using Internal Clock.

2.2 SINE AMPLITUDE

AMPLITUDE: Approximately 1.0VRMS (13dBm) into open circuit, 0.5Vrms (7dBm) into 50 Ω

FLATNESS: +/-3dB from 100Hz to 68MHz referenced to amplitude at 15MHz, stable to +/-1dB from 18-28 $^{\circ}$ C. (-6dB at 50Hz)

2.3 STEP ATTENUATOR

Sine output can be attenuated from 0dB to 60dB in 4dB steps, +/-0.5dB per step. Approx. 0.5Vrms to 500 μ Vrms into 50 Ω

2.4 AC MOS/TTL AMPLITUDE

V_{OL} <0.5V, V_{OH} >3.5V into a 30pF load, series terminated. Rise and Fall Times <5ns. Duty Factor: 45-55%. 50 Ω output impedance. Use series or capacitively-coupled parallel termination.

2.5 CONTROL

Output frequency, phase, sinewave attenuation and clock source are controlled by 7 data bytes in PC I/O address space starting with a base address set by an on-board DIP switch (0338_h default).

2.6 ACCURACY AND STABILITY

Accurate to <+/-10ppm at 18-28 $^{\circ}$ C. Stable to an additional +/-5ppm per year, 18-28 $^{\circ}$ C.

2.7 EXTERNAL CLOCK INPUT

LEVEL: 0.35-2.5Vrms Sine or Square Wave can be applied to the EXT CLK Input BNC. 50 Ω

FREQUENCY: Input range of 5MHz to 30MHz. x6 Multiplier on board.

Internal or external clock selected under software control.

2.8 SPECTRAL PURITY (Typ. 0dB Attenuation)

Phase Noise: <-120dBc, 1kHz offset, 5MHz out.

Spurious: <-60dBc below 10MHz

<-50dBc below 20MHz

<-45dBc below 50MHz

<-40dBc below 68MHz

Harmonic: <-70dBc below 1MHz

<-60dBc below 10MHz

<-50dBc below 20MHz

<-40dBc below 50MHz

<-35dBc below 68MHz

2.9 SWITCHING TIME

NOVATECH INSTRUMENTS, INC. supplied GNU compatible C-language software allows the frequency to be changed in <1ms, depending upon your computer and operating system. The frequency switching time is limited by the ISA bus I/O speed. Attenuation will change in <100ms.

2.10 POWER REQUIREMENTS (from ISA slot)

+5V @ <500mA, -5V @ <50mA.

2.11 SIZE

8-bit ISA bus card with overall length of 200mm, excluding bracket.

2.12 CONNECTORS

BNCs for SINE OUT, AC MOS/TTL OUT and EXT CLK IN.

3.0 HARDWARE INSTALLATION

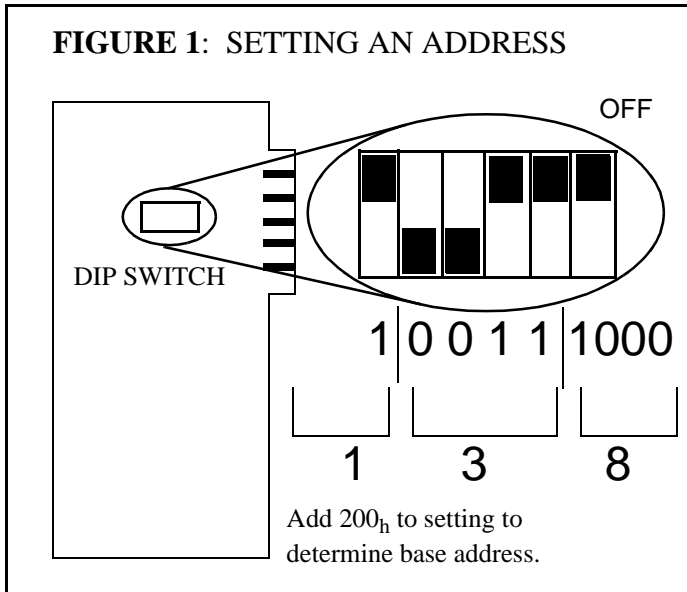
CAUTION:

Opening your computer may expose live voltages. Be sure to follow proper safety precautions.

WARNING:

Before opening your computer or the DDS7pc package, connect the supplied static strap to your wrist and follow the grounding instructions on the strap package. Failure to follow static precautions may damage your computer or the DDS7pc.

3.1 Install the DDS7pc by plugging it into any PC XT, AT or later ISA bus computer. You may use either an 8-bit or 16-bit slot. If the default I/O address selection of 338_h is inappropriate for your configuration, please refer to Figure 1 for information on setting a new address. Allowable address



settings are from 200_h (dip switch setting of 000_h) to 3f8_h (dip switch setting of 1f8_h) in 08_h steps (right most switch).

NOTE:

The DDS7pc does not write data to the PC I/O bus. Incorrect address settings may cause erratic operation of the DDS7pc, but will not affect the operation of your PC.

Any operating system or software which allows control of the ISA bus I/O address space may be

used with this card. See Theory of Operation section for details.

3.2 For best noise performance, locate the DDS7pc as far removed from other cards as possible. This will reduce noise pickup from adjacent cards. Components on the DDS7pc extend up to 15mm from the circuit board. If the DDS7pc is installed in a slot adjacent to another board, verify that no contact is made between the boards, to components or to protruding leads.

4.0 DDS7pc C SOFTWARE

4.1 A C-language program called **dds7pc.c** is provided with the DDS7pc. A compiled version (**dds7pc.exe**) is also provided. This software makes it easy to control the DDS7pc and can be operated in either an Immediate Mode or in a File Mode. In the File Mode, the program executes a sequence of up to 1000 commands from a text file.

4.2 The program is compatible with ANSI C with DOS extensions as implemented in the GNU C compiler “djgpp.” This compiler is available free on the Internet under the GNU “copyleft” agreement. For information regarding this compiler, please follow the link:

<http://www.delorie.com/djgpp/>

A compiled version for older computers (XT, etc.) is found on your distribution disk as **dds7pc8.exe**. Use this for older computers which are not compatible with the 32-bit instructions of the GNU compiler. Any computer with a 386 and newer CPU should not need to use this version.

NOTE:

*For GNU compiles software to run on a DOS PC you must install the DPMS server, **cwsdpms.exe**, in your program execution path. See the above link for details.*

4.3 If you are using software or drivers provided by a third party, please follow the instructions that came with your software.

NOTE:

If you are creating your own software, note that a **RESET** must be provided to the board to initialize the on-board registers. This is accomplished by setting Bit 7 of Address Base+5 Low, then High and returning it Low. See Table 6 for details.

4.4 To install the `dds7pc` program, copy all the files in the DDS7pc subdirectory on the supplied floppy disk to your hard disk. You may also choose to run from the floppy at the expense of speed of execution.

NOTE:

Linux users should see the “readme” file on the distribution disk. Linux operation is somewhat different from the DOS mode.

4.5 To run the `dds7pc` program in Immediate Mode, go to your directory containing the DDS7pc executable files and type “`dds7pc`” or “`dds7pc8`” after the prompt.

4.6 You will then be asked for the DDS7pc base address. If you have not changed the address setting from the factory default of 338_h, then enter 0 (zero) followed by the return or enter key. If you have changed the address, type in that address in Hex, followed by the return or enter key.

4.7 After a short pause while the DDS7pc is initialized, you will be prompted to enter your system clock frequency. If you wish to use the internal DDS7pc clock, type 0 followed by the return or enter key. If you are using an external clock, type in the frequency of your clock. Enter this value as a floating point number in Hz. For example, if you are using a 10.00MHz clock, type: 10.0e6 or 10000000.0 in response to the prompt.

NOTE:

The clock frequency you have typed will be used to calculate the internal settings of the synthesizer. Use as much precision on this input as possible since your output frequency accuracy is determined by this value.

If you have multiple DDS7pc installed, the same external clock must be used on each DDS7pc you

wish to maintain in phase. All DDS7pc connected to the same external clock will remain phase synchronous.

4.8 The DDS7pc will initialize internal settings using the values you have typed in. This takes approximately one second.

NOTE:

If you are using an external clock, that clock must be continuously applied to the DDS7pc as it is used as the internal master clock. If your clock is not applied, you must reset the DDS7pc after the clock is connected. Reset is accomplished at the Frequency input line by typing a **I** in response to the prompt.

4.9 The next prompt asks for output frequency. Type the frequency you would like the DDS7pc to generate and hit the return or enter key. If you enter a frequency that cannot be generated exactly, the `dds7pc` program will set the output to the nearest possible setting. If you are using the internal clock, the setting will be within +/-0.04 Hz.

4.10 You must then set the attenuation of the output signal. You should enter a value from 0 (no attenuation) to 60 (60dB attenuation). Every 4dB of attenuation reduces the output amplitude by 1.585. For example, a 20dB attenuation will reduce the output by 10 (1.585⁵). See Table 1 for output levels. The

Table 1: Nominal Output Levels

Attenuation	Vrms, OC	Vrms, 50Ω	dBm, 50Ω
0	1.00	0.50	7.0
4	0.631	0.315	3.0
8	0.398	0.199	-1.0
12	0.251	0.125	-5.0
16	0.158	0.079	-9.0
20	0.100	0.050	-13.0
24	0.0631	0.0315	-17.0
28	0.0398	0.0199	-21.0
32	0.0251	0.0126	-25.0
36	0.0158	0.0079	-29.0
40	0.0100	0.0050	-33.0

Table 1: Nominal Output Levels

Attenuation	Vrms, OC	Vrms, 50Ω	dBm, 50Ω
44	0.0063	0.0032	-37.0
48	0.0040	0.0020	-41.0
52	0.0025	0.0013	-45.0
56	0.0016	0.0008	-49.0
60	0.0010	0.0005	-53.0

software will automatically round to the nearest value.

4.11 The DDS7pc output frequency and amplitude will change after you have entered the attenuation value. Your output will be maintained until you enter a new setting. You may quit the `dds7pc` program and the setting will remain fixed, provided that your other software and PC do not write to the DDS7pc addresses.

4.12 You may quit the program by entering 0 (zero) at the New Frequency prompt, or by hitting ^C at any time.

4.13 To use the `dds7pc` program in File Mode, you must first create a text file containing a set of DDS7pc commands. You must use an editor or word processor that creates text files with each line terminated by a return. The distribution disk contains a program called "makedds" which can be used to create such a text file. The DDS7pc File Mode commands are listed in Table 2. Table 3 shows an example command file.

4.14 To run the `dds7pc` program in File Mode, go to your directory containing the `dds7pc` program and the command file you wish to run. Type:

```
dds7pc filename
```

4.15 The `dds7pc` program will take several seconds to initialize and adjust to your system speed and then begin executing your command file.

5.0 DDS7pc Theory of Operation

NOTE:

This section provides information on the operation of the DDS7pc. Use this information if you plan to

write your own software or modify the software provided.

5.1 Please refer to the simplified System Block Diagram in Figure 2 for the following discussion.

5.2 The Host computer loads data bytes into 6 write-only 8-bit latches on the DDS7pc. When the DDS7pc hardware detects an I/O write signal on the ISA bus, it decodes the PC address, and if it matches the setting for the DDS7pc, it latches the data from the bus. These 6 data bytes determine the frequency, phase and attenuation settings for the DDS7pc. One additional address is decoded and is used to issue a "NEW_FREQ" command internal to the DDS7pc.

NOTE:

The first command sent to the DDS7pc must be a "RESET." This is accomplished by setting Bit 7 at BASE+5 Low, then High and back Low. This bit must remain low in normal operation.

Never issue a "NEW_FREQ" command without first writing to the Frequency and Phase registers.

5.3 The DDS7pc uses 7 I/O addresses beginning with the Base Address set by the on-board dip switch (switch setting added to 200_h). Table 6 shows the addresses used by the DDS7pc and their function.

NOTE:

The timing on the DDS7pc is asynchronous to the timing on the PC bus and host computer.

5.4 At every cycle of the DDS7pc master clock (either internal or external) the 32-bit DDS (direct digital synthesizer) integrated circuit increments the phase of an internal register by a value determined by the frequency setting loaded by the PC into the on-board registers. This digital phase value is converted to a sine amplitude level and delivered to an on-chip 10-bit digital-to-analog converter. The analog signal from this converter is filtered by a 7th-order elliptical low pass filter, amplified and then sent through a programmable step attenuator to the SINE OUT BNC receptacle.

Table 2

dds7pc FILE MODE COMMANDS

<u>EXAMPLE COMMAND</u>	<u>DESCRIPTION</u>
clock 10.00e6	A record beginning with “clock” followed by a floating point number between 5MHz and 30MHz will set the clock to external and use the value for calculating the internal setting. The external clock is frequency multiplied by 6 to obtain the internal master clock. Do not include this record if you plan to use the internal default clock.
addr 02F0	“Addr” followed by four digits loads the Hex value of the DDS7pc address into the dds7pc Program. The default is 0338 _h and this command is not required to be in the text file unless the DDS7pc address was changed. The example command would use the address 02F0 for the DDS7pc. Do not include this record if you plan to use the default address.
out 1.234e6 12 1.25	“Out” followed by three floating point numbers sets the frequency, attenuation and dwell time. Dwell time delays execution of the next “out” command. A dwell time of 0 will cause a pause until the enter key is hit. When paused use ^C to quit. The example command would set the DDS7pc output to 1.234 MHz; set the DDS7pc attenuation to 12 dB and delay 1.25 seconds before executing the next command. The closest possible setting for attenuation and frequency is used by the program.
start out 1000000.0 12 10 out 10.0e6 24 19 stop	“Out” commands preceded by “start” and followed by “stop” comprise a sweep and will be continually repeated until the user hits a key. The example sequence of commands would set the output to 1MHz and 12dB attenuation and pause for 10 seconds. It would then set the output to 10 MHz and 24 dB attenuation and pause for 19 seconds and then repeat the sequence until a key is hit. All start/stop sequences in the file are executed at least once, while only the last start/stop sequence in the file is repeated. The closest possible setting for attenuation and frequency is used by the program.
reset	Sets Frequency to zero and attenuation to 60 dB.
#	Allows adding comments to a file of commands. The dds7pc program ignores all lines beginning with the # character.

Table 3

dds7pc FILE MODE Example File

```
# Example Text File
clock 10.00e6
addr 02F0
out 1.234e6 12 1.25
start
out 1000000.0 12 10
out 10.0e6 24 19
out 20.0e6 0 5.5
out 22.0e3 60 12
stop
```

This example file sets the DDS7pc to external clock at 10.0MHz and the address to 2F0_h. It then sets the frequency to 1.234MHz, dwells there for 1.25 seconds. A sequence of 4 output frequencies are then executed in a loop, starting with 1.0MHz at 12dB attenuation and 10 seconds dwell. The sequence continues to 10.0MHz with 24dB of attenuation and 19 seconds of dwell, and so on. This loop continuously repeats until interrupted by a key press, or a ^C.

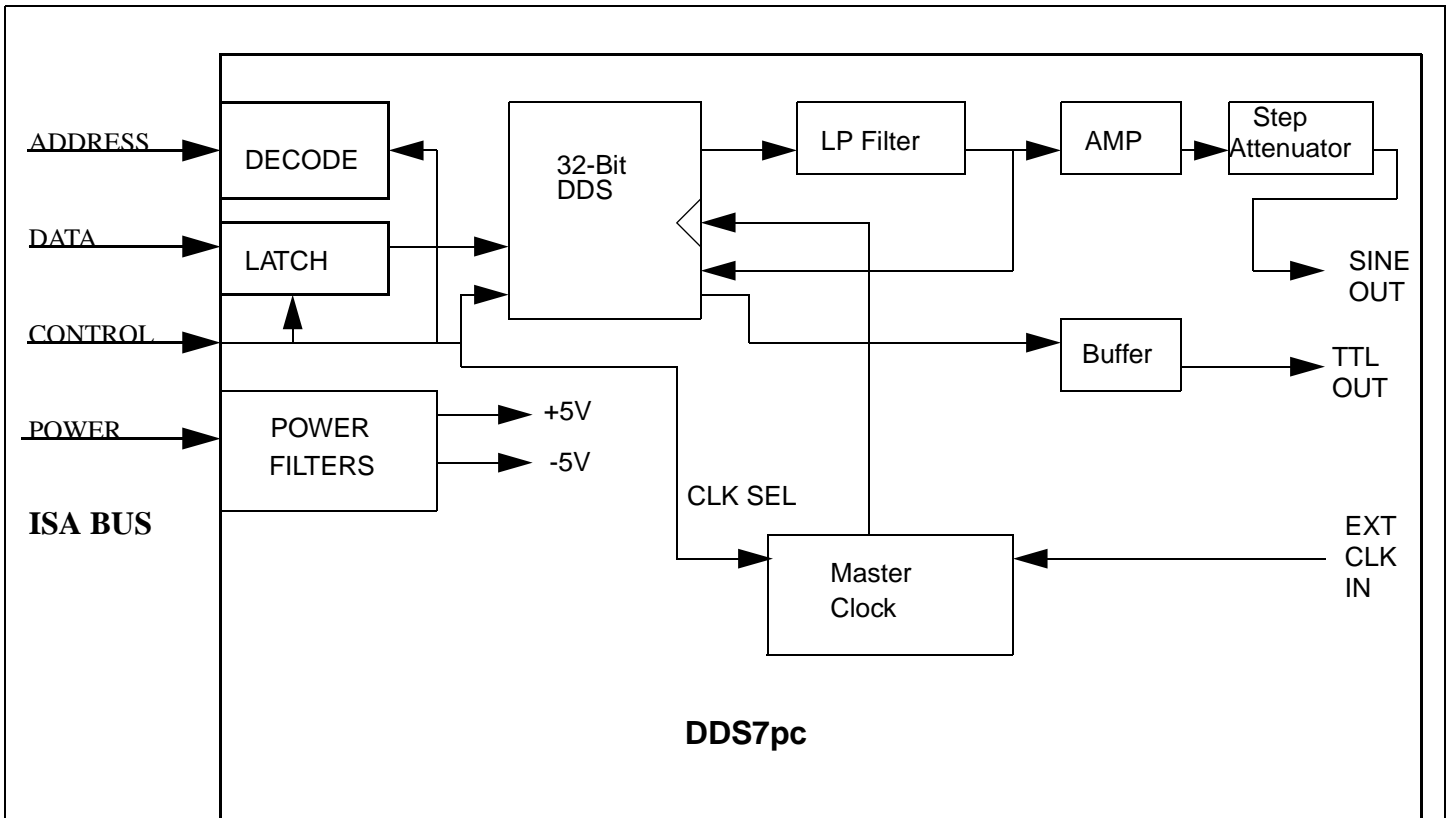


Figure 2

Simplified System Block Diagram

5.5 The filtered sine signal is also sent to an on-chip comparator converting the sine level to an AC MOS/TTL level signal which is then buffered and made available at the AC MOS/TTL OUT BNC receptacle.

5.6 The frequency generated by the DDS IC is determined by the 32-bit frequency word loaded into the frequency register on the DDS7pc. The output frequency is given by:

$$F_{\text{out}} = F_{\text{setting}} * F_{\text{clock}} / 2^{32} \text{ Hz}$$

Where: $F_{\text{clock}} = 171,798,691.840 \text{ Hz}$ (internal)
(or 6x external clock input)
 $F_{\text{setting}} =$ Binary value stored by PC
(F_{setting} ranges from 0 to $2^{32}-1$)

This reduces to:

$$F_{\text{out}} = 0.04 * F_{\text{setting}} \text{ Hz}$$

for the internal (default) clock.

5.7 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the master clock frequency. While it is possible to generate an output near 50% of the clock, the distortion is large. Therefore the output is limited to approximately 40% of the system clock and a steep output filter is provided on board: in this case a 7th-order elliptical low pass filter. The Novatech Instruments, Inc. supplied software automatically limits you to 40% of your clock.

5.8 If you are using an external clock which is substantially lower than 28.6MHz (internal clock divided by 6), you may need to filter the Sine Output to obtain acceptable distortion, depending upon your application requirements. Set the corner frequency at 40% or less of your external clock frequency times 6. The lower your filter as a percentage of your clock frequency, the lower the distortion.

NOTE:

Since this filter occurs before the signal is level shifted to AC MOS/TTL, the AC MOS/TTL output may be erratic or distorted when using low external clock frequencies. If you require a AC MOS/TTL

level signal when using low values of an external clock, it is recommended that you use an external comparator/level shifter connected to the output of your external filter. Contact Novatech Instruments, Inc. if you require application assistance.

5.9 For example, if you are using a 10MHz external clock, the internal clock is 6x this or 60MHz. An optimal filter for this frequency would then be approximately 24MHz (40% of 60MHz). Note that your software distribution disk contains several filter design programs that you may find useful.

6.0 PERFORMANCE TEST

6.1 Install the DDS7pc as directed Section 3 and install the software as instructed in Section 4. You may use the immediate mode to perform the following tests or you can use the text files included on the distribution disk. The File Mode will reduce the time required to perform the test.

6.2 See Table 4 for a list of recommended test equipment to perform the following measurements.

Table 4: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	200MHz, 50Ω	Tektronix, TDS360
RF Probe	100kHz- 70MHz	Tektronix P6420 or HP34301A
DMM	ACRMS, dB	HP34401A
50Ω Termination	50Ω, +/-1%	Tektronix 011- 0049-01 or Pomona 4119- 50
Frequency Counter	100MHz	HP53132A
Counter Time Base	<+/-0.1ppm	Novatech Instruments Model 2950AR

6.3 **Verify Frequency Accuracy.** To verify the frequency of the DDS7pc, set the output sequentially to each value in Table 5. Connect the recommended frequency counter set to 50Ω termination and 1Hz resolution. Verify the limits show in Table 5. You

Table 6

ISA Bus I/O Addresses and their DDS7pc Functions

<u>PC BUS ADDRESS</u>	<u>BUS DATA</u>	<u>DDS7pc Significance</u>
Base +0	Bit 0	Frequency Setting Bit 0 (FS0), LSB
	Bit 1	FS1
	(...)	(...)
	Bit 7	FS7
Base +1	Bit 0	FS8
	Bit 1	FS9
	(...)	(...)
	Bit 7	FS15
Base +2	Bit 0	FS16
	Bit 1	FS17
	(...)	(...)
	Bit 7	FS23
Base +3	Bit 0	FS24
	Bit 1	FS25
	(...)	(...)
	Bit 7	FS31 (MSB)
Base +4	Bit 0	AMP0 (4dB)
	Bit 1	AMP1 (8dB)
	Bit 2	AMP2 (16dB)
	Bit 3	AMP3 (32dB)
	Bit 4	not used
	Bit 5	not used
	Bit 6	not used
	Bit 7	EXTERNAL CLK SELECT (High = External)
Note: A logical low in an amplitude bit means the attenuation is inserted. Add all selected attenuation values to obtain total attenuation.		
Base +5	Bit 0	PS0 (LSB, 11.25° per step)
	Bit 1	PS1
	Bit 2	PS2
	Bit 3	PS3
	Bit 4	PS4 (MSB)
	Bit 5	not used
	Bit 6	not used
	Bit 7	RESET (Low->High->Low = Reset). Must be first.
Base +6	not used	
Base +7	not used	NEW_FREQ Upon a write to this address Frequency and Phase are automatically updated.

Default Base Address is 0338_h. Can be set from 0200_h to 03f8_h (switch: 000_h to 1f8_h).

may use the file mode and the file "table5.txt" to run this test. Test both Sine Out and ACMOS out to verify functionality of both outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. (LSD = Least Significant Digit on counter).

Table 5: Frequency Accuracy Test Points

Frequency	Tolerance
100 Hz	+/-1 LSD
1 kHz	+/-1 LSD
100 kHz	+/-1 Hz +/-1 LSD
1 MHz	+/-10 Hz +/-1 LSD
10 MHz	+/-100 Hz +/-1 LSD
30 MHz	+/-300 Hz +/-1 LSD
68 MHz	+/-680 Hz +/-1 LSD

6.4 Sine Out Amplitude Verification. Set the frequency of the DDS7pc to 10kHz. Connect the DDS7pc to the DMM through a 50Ω feedthrough termination. Set the DMM to AC Volts. Verify a reading of 0.5Vrms +/-0.1Vrms. Remove the 50Ω termination. Verify an amplitude of 1.0Vrms +/-0.2Vrms.

6.5 Output Attenuation Verification. Connect the recommended DMM through a 50Ω feedthrough termination to the Sine Out of the DDS7pc. Set the DDS7pc output to 10kHz, 0dB attenuation. Select the AC volts function on the DMM and then select dB. The meter should read 0dB. Sequentially increase the attenuation by 4dB steps. Verify that the attenuation values of Table 7 are met. Values

Table 7: Attenuation Values

Attenuation	Expected Range, -dB
0	--
4	3.5 to 4.5
8	7.5 to 8.5
12	11 to 13
16	15.5 to 16.5
20	19 to 21
24	23 to 25
28	26.5 to 29.5
32	31.5 to 32.5
36	35 to 37
40	39 to 41

Table 7: Attenuation Values

Attenuation	Expected Range, -dB
44	42.5 to 45.5
48	47 to 49
52	50.5 to 53.5
56	54.5 to 57.5
60	58 to 62

will be negative (representing attenuation) on the DMM. You may use the File Mode and the file "table7.txt" to perform this test. Remove the 50Ω feedthrough termination, reconnect the DMM and reset the attenuation on the DDS7pc to 0dB. Verify that the DMM reads +6dB (+5.5dB to +6.5dB). This verifies the output impedance on the Sine Out receptacle.

6.6 Output Flatness Verification. Verify that the Sine Out is flat with frequency by performing the following test. Connect an RF probe to the DDS7pc terminated with a 50Ω feedthrough termination. Connect the output of the RF probe to the DMM, set to DC Volts. Set the output of the DDS7pc to 15MHz, 0dB attenuation. Select dB on the DMM.

6.7 Using the Immediate Mode, set the DDS7pc to the frequency values of Table 5. Verify that the DMM reading is 0dB +/-3dB (-3dB to +3dB). Exclude frequencies below 100kHz, due to probe limitations.

6.8 ACMOS/TTL Verification. Using a short coaxial cable connect the ACMOS/TTL Out to the recommended oscilloscope set for 50Ω termination. Using the frequency values of Table 5, verify that the output duty factor ranges from a minimum of 45% high and 55% low to a maximum of 55% high and 45% low.

6.9 Set the frequency to 1kHz. Change the termination from 50Ω to 1MΩ on the oscilloscope. Verify that the 50Ω amplitude is 1/2 that of the 1MΩ amplitude, +/-10%.

7.0 CALIBRATION

7.1 The DDS7pc has only three adjustable components. Calibration should only be performed if the DDS7pc fails the performance test or if the unit has

been repaired. Routine adjustments are not recommended nor required. The procedure below assumes that the DDS7pc is out of calibration or has been repaired.

7.2 Install the DDS7pc onto an ISA-bus extender card or an accessible 8-bit slot on your PC. Verify that the voltages delivered by the ISA bus are within tolerance as shown in Table 8. Connect the negative

Table 8: ISA Bus Voltages

Supply	Acceptable Range	Location on DDS7pc
+5 V	+4.75 to 5.5 V	P1 pin 1
-5 V	-5.5 to -4.5 V	P1 pin 3

lead of your DMM to Pin 2 of P1. If these voltages are out of tolerance, then do not proceed with calibration of your DDS7pc. Most PCs will meet these specifications.

NOTE:

Allow the DDS7pc to warm up for at least 15 minutes before performing any adjustments.

7.3 Connect your oscilloscope using a 10x, 500 Ω probe to the base of Q1. Adjust L1 using a non-metallic tuning tool for maximum amplitude. This is a broad adjustment and need not be set exactly. You may also use an RF probe and adjust for maximum DC voltage on your DMM.

7.4 Disconnect your oscilloscope. Set the output of the DDS7pc, using the supplied software, to 1.000MHz, 0dB attenuation. Connect the Sine Output to your frequency counter. Adjust C3 using a non-metallic adjustment tool for 1.0000MHz, +/-2Hz.

7.5 Set the frequency to 10kHz. Connect the output to the DMM set for AC Volts. Do not use a 50 Ω termination. Adjust R52 for 1.00Vrms +/-0.1Vrms.

7.6 This completes the calibration of the Model DDS7pc.

WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

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