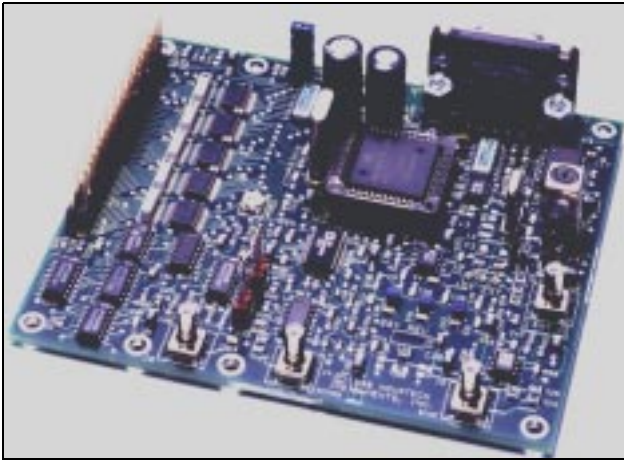


# NOVATECH INSTRUMENTS, INC.

## 68MHz DDS Signal Generator Module Model DDS7m



The DDS7m is a 68MHz Direct Digital Synthesized Signal Generator on a small circuit board. The DDS7m generates both Sine and ACMOS/TTL output signals simultaneously up to 68MHz in 0.04Hz steps under RS232 or binary parallel control. The parallel input allows frequency updates in less than 400ns when using the internal clock. Multiple DDS7m are phase synchronous when driven from the same clock source. The DDS7m has a clock output that allows one unit to drive up to ten other DDS7m in a synchronized multiple phase output system.

### Specifications:

#### OUTPUTS

TYPES: Sine and ACMOS/TTL simultaneously.  
IMPEDANCE: 50 $\Omega$   
RANGE: 100Hz to 68MHz in 0.04Hz steps (int. clock).  
SINE AMPLITUDE: approximately +7dBm (0.5Vrms) into 50 $\Omega$  load.  
FLATNESS: +/-3dB from 100Hz to 68MHz referenced to amplitude at 15MHz, stable to +/-1dB from 18-28  $^{\circ}$ C, 0dB attenuation. (-6dB at 50Hz)  
CLOCK OUTPUT: ACMOS level clock at the oscillator frequency. Will drive up to 10 additional DDS7m when applied to their external clock input. Frequency is equal to External Clock In when External Clock In is used.  
UNFILTERED SINE: Sine output with no filter. Two pin header. 50 $\Omega$

#### ACMOS/TTL AMPLITUDE

$V_{OL} < 0.5V$ ,  $V_{OH} > 3.5V$  into a series terminated 30pF load.  $T_{r,f} < 5ns$ . Duty Factor: 45-55%. 50 $\Omega$

#### CONTROL

Output frequency and phase are controlled either by an RS232 serial port at 19.2kbaud or a binary parallel port. RS232 control allows nonvolatile storage of settings. The parallel port allows frequency/phase updates in <400ns when using the internal clock. Control method is jumper selectable and detected upon power up.

#### ACCURACY AND STABILITY

<+/-10ppm at 18-28  $^{\circ}$ C. Stable to an additional +/-5ppm per year, 18-28  $^{\circ}$ C. (Internal Clock)

#### EXTERNAL CLOCK IN

LEVEL: 0.35-2.5Vrms Sine or Square Wave. 50 $\Omega$   
FREQUENCY: 5MHz to 30MHz. x6 Multiplier on board. (May require external filter for optimum performance.)

#### SPECTRAL PURITY (Typ. 50 $\Omega$ load, internal clock)

Phase Noise: <-120dBc, 10kHz offset, 5MHz out.  
Spurious: <-60dBc below 10MHz (typ. 200MHz span)  
<-50dBc below 20MHz  
<-45dBc below 50MHz  
<-40dBc below 68MHz  
Harmonic: <-70dBc below 1MHz  
<-60dBc below 10MHz  
<-50dBc below 20MHz  
<-40dBc below 50MHz  
<-35dBc below 68MHz

#### SWITCHING TIME

Parallel Control: Output changes in <400ns from frequency trigger. RS232 control depends upon host speed and commands sent, typ. <10ms for a new frequency.

#### POWER REQUIREMENTS

4.75 to 5.25V @ <350mA and -5.25 to -4.75V @ <100mA.

#### SIZE

88.9mm by 101.6mm circuit board. Max. height 19mm.

#### CONNECTORS

SMB for Sine, ACMOS/TTL, CLK OUT and EXT CLK IN. 3-pin header for Power. 40-pin header for parallel in.