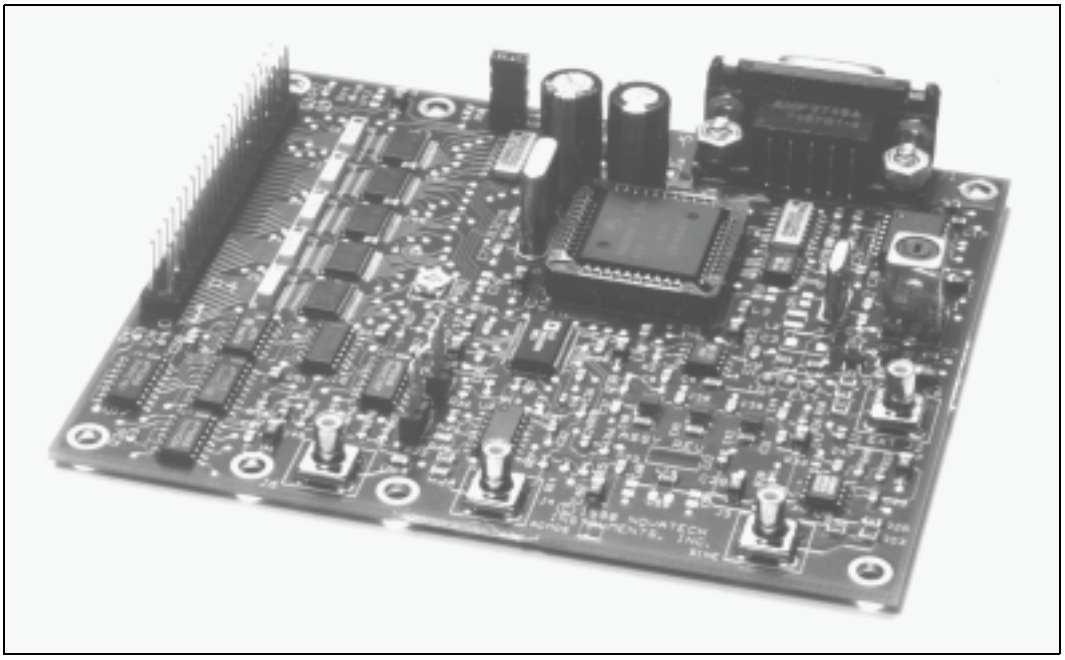
NOVATECH

INSTRUMENTS, INC.

INSTRUCTION MANUAL
Model DDS7m 68MHz DDS Signal Generator Module



DDS7m

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1.0 DESCRIPTION

1.1 The Model DDS7m is a 68MHz **D**irect **D**igital **S**ynthesizer (DDS) on a small printed wiring module with both parallel and RS232 serial control. The DDS7m provides both Sine and ACMOS output signals, which can be set from 100Hz to 68MHz in 0.04Hz steps when using the internal clock.

1.2 The DDS7m can also be used with an External Clock input. An on-board x6 frequency multiplier generates the master clock allowing user configured frequency ranges. When used with an external clock, multiple DDS7m are phase synchronous. When using an external clock, customer supplied filters may be required for optimum performance. The Clock Out from one DDS7m can be used as an external clock source for multiple DDS7m.

2.0 SPECIFICATIONS

2.1 OUTPUTS
TYPES: Sine and ACMOS/TTL Simultaneously.
IMPEDANCE: 50 Ω.
FREQUENCY: 100Hz to 68MHz in 0.04Hz steps, using Internal Clock.
CLOCK OUTPUT: ACMOS level clock at the oscillator frequency. Will drive up to 10 additional DDS7m when applied to their external clock input. Equal to Ext. Clk. In when Ext. Clk. In is used.
UNFILTERED SINE: Sine output with no filter. Two pin header. 50Ω.

2.2 SINE AMPLITUDE
AMPLITUDE: Approximately 0.5Vrms (7dBm) into 50 Ω.
FLATNESS: +/-3dB from 100Hz to 68MHz referenced to amplitude at 15MHz, stable to +/-1dB from 18-28 ^{o}C. (-6dB at 50Hz)

2.3 ACMOS/TTL AMPLITUDE
V_{OL}<0.5V, V_{OH}>3.5V into a 30pF load, series terminated. Rise and Fall Times <5ns. Duty Factor: 45-55%. 50 Ω output impedance. Use series or capacitively-coupled parallel termination.

2.4 ACCURACY AND STABILITY
Accurate to <+/-10ppm at 18-28 ^{o}C. Stable to an additional +/-5ppm per year, 18-28 ^{o}C.

2.5 EXTERNAL CLOCK INPUT
LEVEL: 0.35-2.5Vrms Sine or Square Wave can be applied to the EXT CLK Input SMB. 50 Ω.
FREQUENCY: Input range of 5MHz to 30MHz. x6 frequency multiplier on board.

2.6 SPECTRAL PURITY (Typ. 50Ω load, int clk.)
Phase Noise: <-120dBc, 10kHz offset, 5MHz out.
Spurious: <-60dBc below 10MHz (200MHz span)
<-50dBc below 20MHz
<-45dBc below 50MHz
<-40dBc below 68MHz
Harmonic: <-70dBc below 1MHz
<-60dBc below 10MHz
<-50dBc below 20MHz
<-40dBc below 50MHz
<-35dBc below 68MHz

2.7 CONTROL
Output Frequency and phase are controlled either by an RS232 serial port at 19.2 kbaud or a parallel binary port. RS232 control allows non-volatile storage of settings. The parallel port allows frequency and phase updates in <400ns when using the internal clock. Control method is jumper selectable and detected upon power up.

2.8 SWITCHING TIME
Parallel Control: Output changes in <400ns from frequency trigger. RS232 control depends upon host speed and commands sent, typically <10ms for a new frequency.

2.9 POWER REQUIREMENTS
+4.75 to 5.25V @ <350mA; -5.25 to -4.75V @ <100mA.

2.10 SIZE
88.9mm by 101.6mm card. Max. height: 19mm.

2.11 CONNECTORS
SMBs for SINE, ACMOS/TTL, CLK OUT and EXT CLK IN. 3-pin Header for power. 40-pin for Parallel Control.

3.0 HARDWARE INSTALLATION

WARNING:

The DDS7m contains static sensitive components. Before opening the package, follow appropriate static precautions. Failure to follow static precautions may damage the DDS7m.

3.1 **Power Connection.** Figure 1 shows a top view of the DDS7m module. The required power of +/- 5Vdc is applied through a 3-pin connector (mates with Amp 640621-3). If you are using Novatech supplied wires, connect your +5v supply to the RED wire; your -5v supply to the BLUE wire and their common-connected returns to the BLACK wire.

3.2 The quality of your power supply may affect the performance of the DDS7m. The supply should be free of ripple and noise (<50mV). Even though extensive filtering is used on the DDS7m board, a quiet and well regulated power supply will ensure optimum performance. If switching power supplies are used, please verify that your system noise requirement is met.

3.3 **RS232 Installation.** To use the DDS7m in the RS232 mode, verify that the jumper W3 is installed before power-up and connect your host computer to the 9-pin female RS232 connector on the DDS7m. If you are using a PC, a 9-pin monitor extension cable will allow direct connection to the DDS7m without the use of a null modem cable or gender changer. If you are using a different computer, terminal or other control source, please note that the data **TO** the DDS7m is on pin 3; the data **FROM** the DDS7m is on pin 2 and the **COMMON** return is on pin 5. Set your host to 19.2 kbaud, 8 bits, 1 stop bit, no parity and no hardware flow control. See Table 1 for RS232 Commands.

Table 1: RS232 Commands

RS232 Command	Function
F XX.XXXXXXXX	Set Frequency in MHz. Software sets to nearest 0.04Hz. Decimal point required.
E D	Echo Disable
E E	Enable Echo
R	Reset

Table 1: RS232 Commands

RS232 Command	Function
P N	Set Phase. N is an integer from 0 to 31. Phase is set to N*11.25^{o} (N*Pi/16 radians)
A E	ACMOS/TTL Enable
A D	ACMOS/TTL Disable (output set low)
SAVE	Save current output. Used as default upon next power up.
QUE	Return last saved frequency, phase and status.

3.4 The commands are not case sensitive. There must be a space after each command except R, SAVE and QUE. End with any combination of CR, LF or CRLF

3.5 Table 2 shows the RS232 error codes.

Table 2: RS232 Error Codes

Error Code	Meaning
OK	Good command received (not sent for R and QUE)
?0	Unrecognized Command
?1	Bad Frequency
?2	(Not Used, Reserved)
?3	Input line too long
?4	Bad Phase

NOTE:

The frequency setting is rounded to the nearest LSB (0.04Hz with default clock) output when using the RS232 control port.

3.6 The "QUE" command returns a string of the form "017D7840 00 A:E E:E". The first number is the binary frequency setting in Hexadecimal (Hex); multiply by 0.04Hz to obtain output frequency. The next number is the phase setting in Hex. The next two terms show status of the A and E commands. Note that the frequency will be scaled as discussed below if an external clock is used.

3.7 **Parallel Installation.** The DDS7m can also be controlled by a parallel binary connection made to the 40-pin (20x2) header. See Table 3 for connector

Figure 1: Connection Placement Diagram

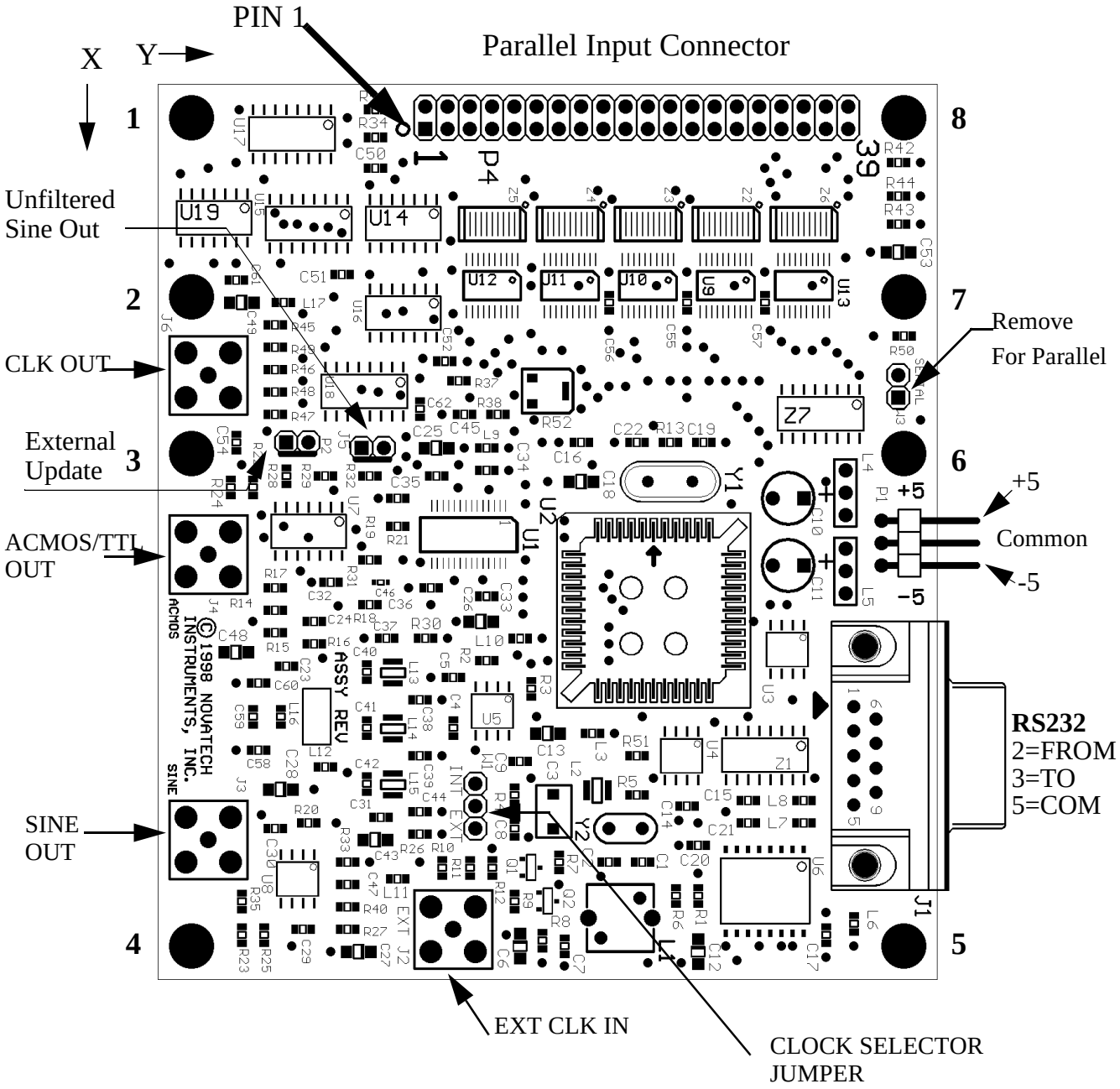

Table 3: Parallel Connector Pinout

Pin Number	Function	Pin Number	Function
1	Frequency Select 1 (FS1)	2	Frequency Select 0 (FS0)
3	FS3	4	FS2
5	FS5	6	FS4
7	FS7	8	FS6
9	FS9	10	FS8
11	FS11	12	FS10
13	FS13	14	FS12
15	FS15	16	FS14
17	FS17	18	FS16
19	FS19	20	FS18
21	FS21	22	FS20
23	FS23	24	FS22
25	FS25	26	FS24
27	FS27	28	FS26
29	FS29	30	FS28
31	FS31 (MSB)	32	FS30
33	PS3	34	Phase Select 4 (PS4) (MSB)
35	PS1	36	PS2
37	NEW_FRQ-	38	PS0
39	Circuit Common (ground)	40	BUSY- (output)

Table 4: Mounting Hole Locations

Hole Number	Location (x,y) mm
1	3.81, 3.81
2	24.13, 3.81
3	41.91, 3.81
4	97.79, 3.81
5	97.79, 85.09
6	41.91, 85.09
7	24.13, 85.09
8	3.81, 85.09

Figure 2: Parallel Input Timing Diagram (Not to Scale)

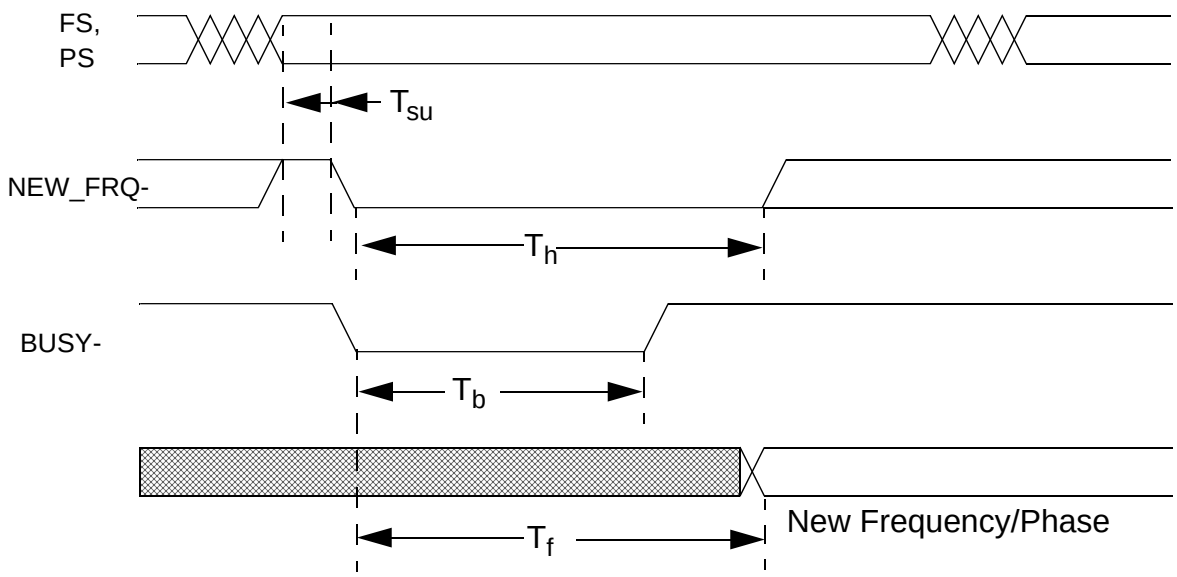

Table 5: Parallel Control Timing

Parameter	Name	Min	Max	Notes
T_{su}	Data Setup Time	25ns	--	
T_h	New Frequency Select Hold Time	25ns	--	
T_b	Busy Time		280ns	finishes in 8 master clock cycles, values shown for internal clock
T_f	New Frequency Update Time		385ns	finishes in 11 master clock cycles, value shown for internal clock

pinout and pin descriptions. For parallel operation, W3 must be removed before power is applied.

NOTE:

For maximum interface speed, the parallel inputs do not have additional protection against ESD damage beyond that provided by the CMOS inputs (+/-2kV, Human Body Model. +/-200 V, machine model).

3.8 All of the inputs, **FS0-31, PS0-4** and **NEW_FRQ-** are VHC CMOS compatible and require:

V_{il} <= 0.3*V_{cc} (nominally 1.5 volts)

V_{ih} >= 0.7*V_{cc} (nominally 3.5 volts)

3.9 C_{in} on each pin is approximately 12pF (application cable capacitance not included). All the input pins are pulled to V_{cc} via a 10kΩ resistor. It is recommended that a series termination resistor of 50-100Ω be used in each signal line to prevent reflections and ringing. The exact value will be determined by your application circuitry and cabling.

3.10 **BUSY-** is a VHCMOS compatible output with:

V_{oh} >= 4 V (I_{load} <= -100μA)

V_{ol} <= 0.2V (I_{load} <= 100μA)

3.11 **BUSY-** going HIGH indicates that all parallel data has been loaded into the DDS circuitry. Some latency remains before the output frequency is updated. Please refer to the timing diagram, Figure 2, for details.

3.12 **BUSY-** has a series resistance of 500Ω to prevent damage due to accidental shorts. If this output is used for handshaking be sure to account for capacitive loading on this signal.

3.13 Please refer to the timing diagram, Figure 2, and Parallel Control Timing, Table 5, for the details on setting frequency and phase when using the parallel interface.

3.14 **Internal Clock.** If you plan to use the DDS7m internal clock, verify that the clock select jumper wire is in the INT position and that the External Clock Input is left unconnected (the jumper is a short piece of #28 AWG bare wire).

3.15 **External Clock**. If you are providing your own clock source, move the clock select jumper to the EXT position. Apply your clock to the External Clock Input SMB. Note that phase noise and stability are dependent upon your supplied clock. See specifications for signal levels required and acceptable frequency range.

NOTE:

The DDS7m detects "no-clock" and goes into a power down mode. If the clock signal is removed or interrupted during operation, the power much be cycled to reset the DDS7m. If you are using the Serial Control Mode you need only to send a "R" command.

NOTE:

When using an external clock, frequency scaling of the "F" command is required. Please see Operation, Section 4, for details.

3.16 **Signal Outputs.** There are three signal outputs on the DDS7m: Sine, ACMOS/TTL, and Unfiltered Sine. The Sine and ACMOS/TTL are provided on SMB connectors on the board edge. Simply connect your 50Ω application cable to appropriate output. If you are not using the ACMOS/TTL output, it is suggested that it be disabled (only with RS232 control). The Unfiltered Sine is provided on a two-pin header for those applications requiring special filtering.

3.17 The DDS7m also has a CLOCK OUT which can drive up to 10 other DDS7m External Clock inputs. With no load, this output is a VHCMOS (5Vpp) square wave. As it is fanned out to other DDS7m, the amplitude will decrease, but still have adequate signal level for the external input of up to 10 secondary DDS7m. This clock output should be used when multiple DDS7m are required to be synchronized. One DDS7m is then used as a master, using its internal clock. The secondary DDS7m are then connected to the clock output on the master. All DDS7m connected in this way will remain phase synchronous.

3.18 If an exact phase relationship is required among phase synchronous DDS7m operated in the Serial Control Mode, the External Update must be used. All modules should be sent the appropriate set

of commands to establish frequency and phase. Then a high-going pulse of 25ns minimum at ACMOS levels is applied to the External Update connector. This pulse will load all values simultaneously and the parameters set prior to the pulse will remain stable until the next update from the serial control port.

3.19 Exact phase relationships in the Parallel Control Mode are maintained by applying appropriate frequency and phase data to all units and then sending a single NEW_FRQ- pulse to all units.

3.20 **Mounting.** Eight Mounting holes are provided on the board. These holes are electrically connected to circuit common and may be used for shield connections. Clearance is provided for up to 3mm diameter screws. Please allow at least 3 mm clearance on the bottom side when mounting to a conductive chassis or case.

4.0 Operation

4.1 **Power on reset.** After power is applied, the DDS7m takes approximately three seconds to initialize. Commands sent during this time will be ignored or may cause erroneous operation.

4.2 **Serial Mode.** After the DDS7m has been installed in the customer application system, all that is required is to send the appropriate commands. In the RS232 mode, only serial commands need be sent to the module after the power is applied.

4.3 The user host computer software must properly format the serial commands. Incorrect formatting will result in an error code being returned. See Table 2 for a list of RS232 error codes.

4.4 If you are using an external clock, the value sent to the DDS7m during the "F" command must be scaled. The output frequency of the DDS7m when used with an external clock is given by:

$$F_{out} = (F_{command})*(F_{ext\ clk}/F_{int\ clk})$$

4.5 The nominal Internal Clock has a value of 28,633,115.3067 Hz.

4.6 For an example, suppose an external clock of 10.000MHz is used and an output of 1.544MHz is desired:

$$F_{command} = (1.544)*(28.6331153067/10.0000$$
$$= 4.42095303$$

4.7 The command then sent to the DDS7m for the 1.544MHz output, with a 10MHz external clock, will be:

```
F 4.42095303
```

NOTE:

You must account for your clock frequency error and calculation roundoff when using an external clock and the serial mode.

4.8 **Parallel Mode.** When the parallel mode is chosen, the operation of the DDS7m is dependent upon the user supplied interface circuitry. The on-board microprocessor and software are disabled in parallel operation. Therefore, no error conditions are detected or reported.

4.9 As in the serial mode, the use of an external clock scales the frequency output of the DDS7m. In this case, however, it is more constructive to look at the binary value of the frequency setting. Since the user sets the binary value of FS0-FS31 (value of 0 to 2^{32}-1), the use of the external clock scales the value of the LSB. Using the 10MHz example of the serial mode description:

$$F_{out} = 0.04*F_{setting}\ F_{ext}/F_{int}\ Hz$$
$$F_{out} = 0.013970*F_{setting}\ Hz$$

4.10 Note that values greater than 2^{31}-1 violate Nyquist (see theory of operation).

5.0 Theory of Operation

5.1 Please refer to the simplified System Block Diagram in Figure 3 for the following discussion.

5.2 At every cycle of the DDS7m master clock (either internal or external) the 32-bit DDS integrated circuit increments the phase of an internal register by a value determined by the frequency setting loaded into the on-chip registers. This digital

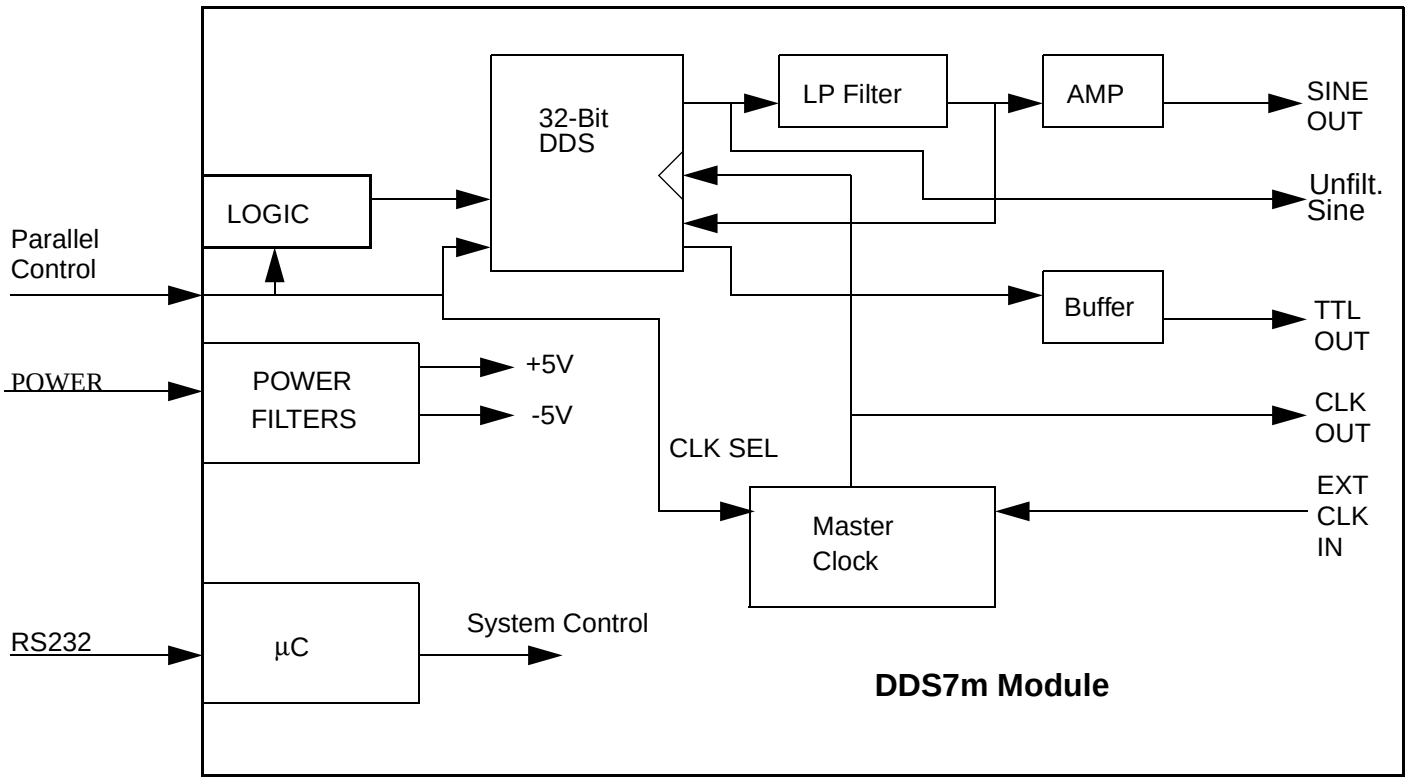

Figure 3
Simplified System Block Diagram

phase value is converted to a sine amplitude level and delivered to an on-chip 10-bit digital-to-analog converter. The analog signal from this converter is filtered by a 7th-order elliptical low pass filter, amplified and sent to the SINE OUT SMB receptacle.

5.3 The filtered sine signal is also sent to an on-chip comparator converting the sine level to an ACMOS/TTL level signal which is then buffered and made available at the ACMOS/TTL OUT SMB receptacle.

5.4 The frequency generated by the DDS IC is determined by the 32-bit frequency word loaded into the frequency register on the DDS7m. The output frequency is given by:

$$F_{out} = F_{setting} * 6.0 * F_{clock} / 2^{32} \text{ Hz}$$

Where: F_{clock} = 28,633,115.3067 Hz (internal)
$F_{setting}$ = Binary value stored in DDS IC.
($F_{setting}$ ranges from 0 to 2^{32}-1)

This reduces to:

$$F_{out} = 0.04 * F_{setting} \text{ Hz}$$

for the internal (default) clock.

5.5 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the master clock frequency (2^{31}-1). While it is possible to generate an output near 50% of the clock, the distortion may be unacceptable. Therefore, the output is limited to approximately 40% of the system clock and a steep output filter is provided on board: in this case a 7th-order elliptical low pass filter.

5.6 If you are using an external clock which is substantially lower than 28.633MHz (internal clock), you may need to filter the Sine Output to obtain acceptable distortion for your application. For best performance, set the corner frequency at 40% or less of your external clock frequency times six. The lower your filter as a percentage of your clock frequency, the lower the distortion.

NOTE:

Since this filter occurs before the signal is level shifted to ACMOS/TTL, the ACMOS/TTL output may be erratic or distorted when using low external clock frequencies. If you require a ACMOS/TTL level signal when using low values of an external clock, it is recommended that you use an external comparator/level shifter connected to the output of your external filter. Contact Novatech Instruments, Inc. if you require application assistance.

5.7 For example, if you are using a 10MHz external clock, the internal clock is 6x this or 60MHz. An optimal filter for this frequency would then be approximately 24MHz (40% of 60MHz).

6.0 PERFORMANCE TEST

6.1 Install the DDS7m as directed Section 3. Connect your host controller and operate the DDS7m per Section 4.

NOTE:

Allow the DDS7m to warm up for at least 15 minutes before performing any measurements. The DDS7m should be verified in its installed environment.

6.2 See Table 6 for a list of recommended test equipment to perform the following measurements.

Table 6: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	200MHz, 50Ω	Tektronix, TDS360
RF Probe	100kHz-70MHz	Tektronix P6420 or HP34301A
DMM	ACRMS, dB	HP34401A
50Ω Termination	50Ω, +/-1%	Tektronix 011-0049-01 or Pomona 4119-50
Frequency Counter	100MHz	HP53132A
Counter Time Base	<+/-0.1ppm	Novatech Instruments Model 2950AR

6.3 **Verify Frequency Accuracy.** To verify the frequency of the DDS7m, set the output sequentially to each value in Table 7. Connect the recommended frequency counter set to 50Ω termination and 1Hz resolution. Verify the limits show in Table 7. Test both Sine Out and ACMOS out to verify functionality of both outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. (LSD = **L**east **S**ignificant **D**igit on counter).

Table 7: Frequency Test Points

Frequency	Tolerance
100 Hz	+/-1 LSD
1 kHz	+/-1 LSD
100 kHz	+/-1 Hz +/-1 LSD
1 MHz	+/-10 Hz +/-1 LSD
10 MHz	+/-100 Hz +/-1 LSD
30 MHz	+/-300 Hz +/-1 LSD
68 MHz	+/-680 Hz +/-1 LSD

6.4 **Sine Out Amplitude Verification.** Set the frequency of the DDS7m to 10kHz. Connect the DDS7m to the DMM through a 50Ω feedthrough termination. Set the DMM to AC Volts. Verify a reading of 0.5Vrms +/-0.05Vrms. Remove the 50Ω termination. Verify an amplitude of 1.0Vrms +/-0.1Vrms.

6.5 **Output Flatness Verification.** Verify that the Sine Out is flat with frequency by performing the following test. Connect an RF probe to the DDS7m terminated with a 50Ω feedthrough termination. Connect the output of the RF probe to the DMM, set to DC Volts. Set the output of the DDS7m to 15MHz. Select dB on the DMM.

6.6 Set the DDS7m to the values of Table 7. Verify that the DMM reading is 0dB +/-3dB. Exclude frequencies below 100kHz, due to probe limitations.

6.7 **ACMOS/TTL Verification.** Using a short 50Ω coaxial cable, connect the ACMOS/TTL Out to the recommended oscilloscope set for 50Ω termination. Using the values of Table 7, verify that the output duty factor ranges from a minimum of 45% high and 55% low to a maximum of 55% high and 45% low.

6.8 Set the frequency to 10kHz. Change the termination from 50Ω to 1MΩ on the oscilloscope. Verify that the 50Ω amplitude is 1/2 that of the 1MΩ amplitude, +/-10%.

7.0 CALIBRATION

7.1 The DDS7m has only three adjustable components: L1, C3 and R52. Calibration should only be performed if the DDS7m fails the performance test or if the unit has been repaired. Routine adjustments are not recommended nor required. This procedure assumes that the DDS7m has failed the performance test or has been repaired.

NOTE:

Allow the DDS7m to warm up for at least 15 minutes before performing any adjustments. The DDS7m should be calibrated in its installed environment.

7.2 **Frequency Pre-adjust, L1.** Connect your oscilloscope using a 10x, 500Ω probe to the base of Q1. Adjust L1 using a non-metallic tuning tool for maximum amplitude. This is a broad adjustment and need not be set exactly. You may also use an RF probe and adjust for maximum DC voltage on your DMM.

7.3 **Frequency Adjust, C3.** Disconnect your oscilloscope. Set the output of the DDS7m to 1.000000MHz. Connect the Sine Output to your frequency counter. Adjust C3 using a non-metallic adjustment tool for 1.000000MHz, +/-2Hz.

7.4 **Amplitude Adjust, R52.** Set the frequency to 10kHz. Connect the output to the DMM set for AC Volts. Do not use a 50Ω termination. Adjust R52 for 1.00Vrms +/-0.05Vrms.

7.5 This completes the calibration of the Model DDS7m.

WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

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