NOVATECH
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Variable Pulse Width Generator Option for 409B

AN003

Introduction:

The Model 409B provides four synchronized sinewave outputs which can be independently controlled in frequency and phase. The frequency of each channel is programmable with 32-bits of resolution (0.1Hz using default clock) and phase can be controlled with 14-bits of resolution (0.022^{o}). These features can be used to generate a variable pulse width (variable symmetry) clock output waveform. The Model 409B/01 implements this function internally.

Setting the Pulse Width:

The method is to use two output channels, set to the same frequency, to generate SET and RESET pulses for an S/R (Set/Reset) flip-flop (F/F). By varying the phase of the two channels, the time from SET to RESET is made variable. This allows, at a given repetition rate (frequency), a specific pulse width to be set. At the positive-going zero crossing of the SET signal, the output of the F/F is set to a logic high. The output is returned to a logic low at the positive-going zero crossing of the RESET signal.

For example, suppose a repetition rate of 1MHz is desired and 250ns positive going pulse width is required. If the positive going edge of one channel is used to set the flip-flop, then the positive going edge of the second channel, used to reset the flip-flop, must occur 250ns later. Since 250ns corresponds to 25% of the complete cycle, the phase on the RESET channel should set to lag the SET in phase by 25%. The 409B has a phase command that allows settings of 0 to 16,383. This would correspond to a phase setting of 4096 (rounded) to achieve 25%. Since the RESET channel must lag, the SET channel is programmed to 4096, which is a 250ns lead. (Note that a setting of 50%, or 8192, will give a square wave.) This fractional period relationship holds for all frequencies. Once your rate is chosen, you only need to find the fraction of a period of your desired pulse width.

The instrument requires that the outputs be phased aligned, so the `"M a"` mode must be used. In the 490B/01, the RESET signal is derived from Channel 2 and the SET from Channel 3.

Examples:

The command sequence to set this 1MHz example is:

```
M a
F2 1.00
F3 1.00
P2 0
P3 4096
```

The output from a Novatech Instruments 409B/01 programmed with this sequence is shown below in Figure 1. This is the PECL output, terminated into 50Ω on a Tektronix 3032B Oscilloscope.

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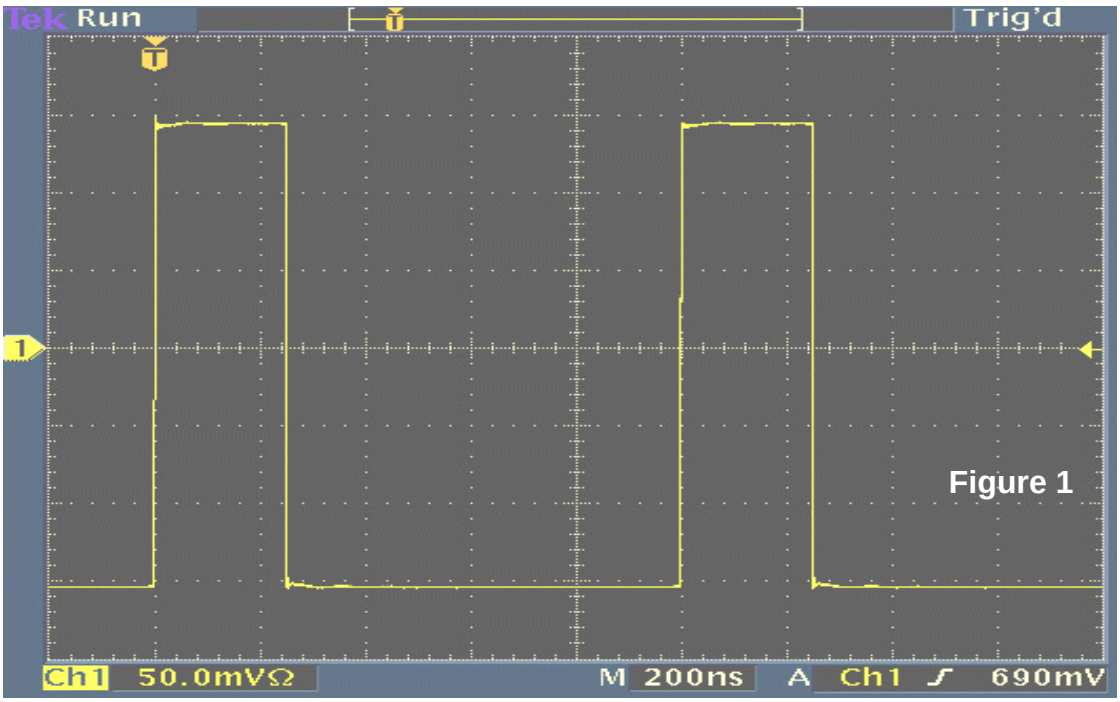
Figure 1: 1MHz, 25% duty cycle.



Operating Notes:

The inputs on the internal pulse width generator board are shaped by third-order Bessel filters (maximally flat delay) followed by high-speed comparators. Due to the propagation delays of the logic used, the minimum practical pulse width is approximately 2ns, with a maximum repetition rate of 50MHz. The inputs are DC-coupled, so the low frequency end is not limited. Note, however, that the sine wave outputs are set by a 10-bit DAC. At very low rates, the comparators will detect the output amplitude granularity, contributing to jitter.

See Figure 2 for an example at a 1kHz rate and 100µs pulse width. The oscilloscope is triggered on the rising edge and the persistence is set to 5s, so the falling edge displays the peak-to-peak jitter of approximately 1µs, or 0.1% of the total period.

The lowest output frequency with the 409B/01 is 0.1Hz. At this rate, the output will be essentially unchanging within the bandwidth of the high-speed comparators and logic used on the board. This could allow noise to trip the pulse width cell, generating false widths. It is recommended that higher repetition rates be used whenever possible. Hysteresis of 10mV is used to increase noise immunity.

Very low duty cycles (or very high) require that the comparators resolve only a few mV of difference between the two sine wave inputs. While it is possible to resolve changes of pulse width on the order of 10 picoseconds, noise considerations may limit the accuracy of these settings. Settings that change the output by 1 or 2%, with a range of 2% to 98% duty cycle, are indicated.

While not a substitute for a full-featured pulse generator, the 409B/01 is suitable for variable pulse width clock applications.

Figure 2: 1kHz rate, with 100µs pulse width.

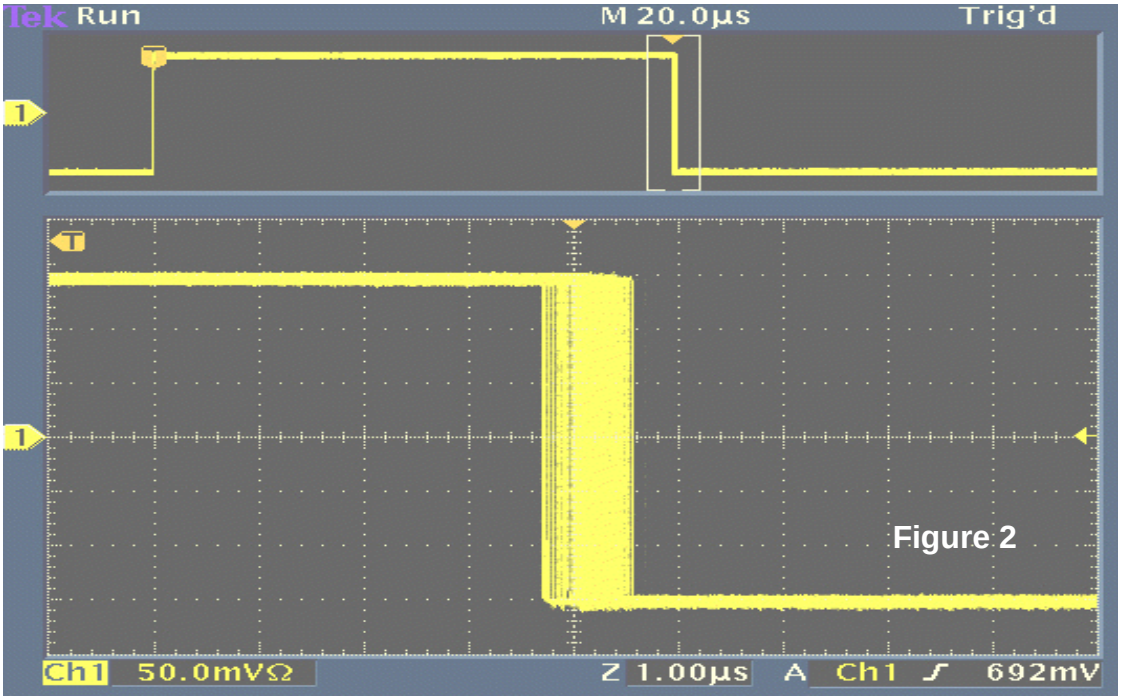
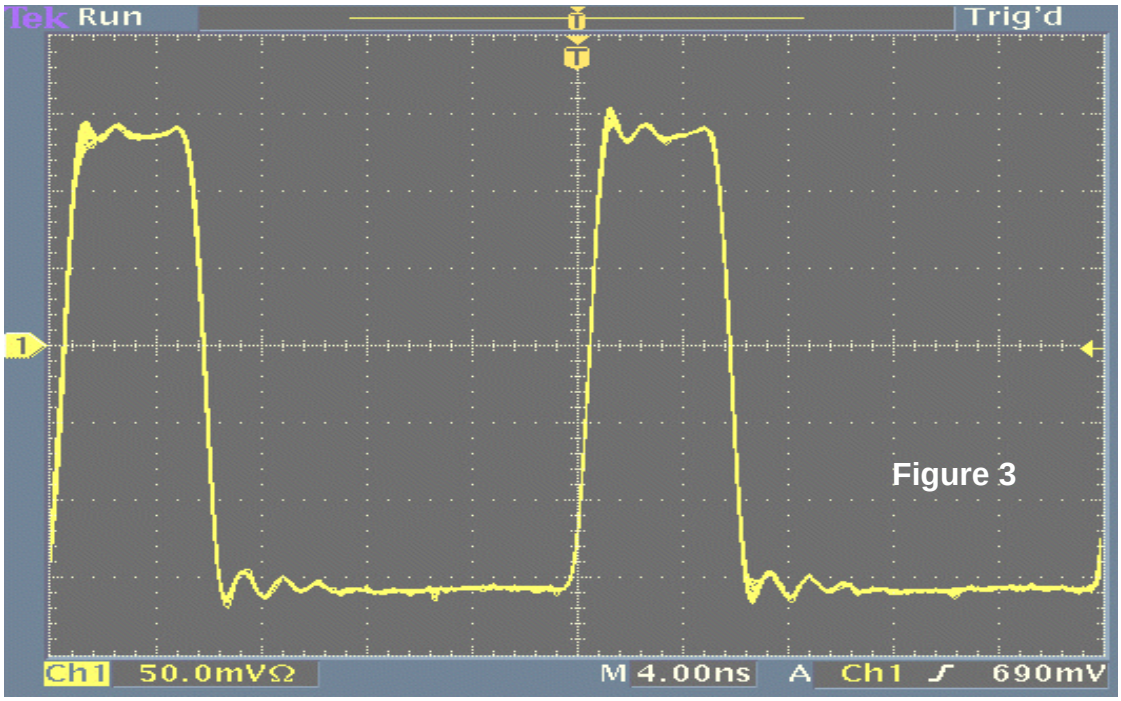


Figure 3 below shows the output at 50MHz and 25% duty cycle.



409B/01 Supplemental Specifications:

Repetition Rate (Frequency):	0.1Hz to 50MHz in 0.1Hz steps (internal clock).
Pulse Width:	Programmable from 0/16384 to 16383/16384 of period with a minimum of 2ns (positive or negative going).
Rise/Fall Times:	<1.5ns into 50Ω (PECL typically <500ps).
Output Levels (Typical):	PECL: 600mVpp OC (300mVpp 50Ω). ACMOS: 3Vpp OC (1Vpp 50Ω).
Output Impedance:	50Ω.

Note that the sine outputs on the 409B Channel 2 and Channel 3 BNCs are replaced by the ACMOS and PECL outputs on the 409B/01.

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