

# NOVATECH INSTRUMENTS, INC.

## Precision 350 MHz Signal Generator Model 425A



The 425A is a Precision 350 MHz Frequency and Phase Agile Synthesized Signal Generator in a small shielded table top case. The 425A generates Sine, LVCMOS, and LVDS output signals simultaneously up to 350 MHz in 10  $\mu$ Hz steps under control from a serial port. Multiple 425A can be synchronized and used to generate the signals needed for radar, acoustic testing and similar applications. The 425A comes with a  $\pm 1.5$ ppm on-board TCXO clock. When locked to a 10.0 MHz external reference, the 425A has the same accuracy and stability as the reference and remains phase synchronous with other units locked to the same reference.

### Specifications:

#### OUTPUTS

TYPES: Sine, LVDS and LVCMOS simultaneously.  
IMPEDANCE: 50  $\Omega$ .  
RANGE: 100 kHz to 350 MHz with 10  $\mu$ Hz resolution (internal clock only).  
SINE AMPLITUDE: approximately +7 dBm (0.5 Vrms) into 50  $\Omega$  load. 14-bit DAC.

#### LVCMOS AMPLITUDE

$V_{OL} < 0.5$  V,  $V_{OH} > 2.0$  V into a series-terminated load.  
 $T_{r,f} < 2.5$  ns. Duty Factor: 45-55%. 50  $\Omega$ . Programmable 16-bit divider with a selectable /2 prescaler allows LVCMOS outputs to less than 10 Hz. (LVCMOS optimized for frequencies  $\leq 125$  MHz)

#### LVDS AMPLITUDE

Meets EIA-644A specifications when terminated into a 100  $\Omega$  differential load (driver: SN65LVDS100, or equivalent).

#### CONTROL

Output frequency (48-bits), phase (14-bits), and scaling (10-bits) are controlled by a serial port. Settings can be saved in EEPROM.

#### ACCURACY AND STABILITY

Accuracy:  $< \pm 1.5$ ppm at 10-40  $^{\circ}$ C. Stable to an additional  $\pm 2$ ppm per year, 18-28  $^{\circ}$ C.

#### EXTERNAL CLOCK IN

LEVEL: 0.25-1.0 Vrms Sine or Square Wave. 50  $\Omega$ .

Phase locked to 10 MHz (lock range is typically  $\pm 10$ ppm).

#### SPECTRAL PURITY (Typ. 50 $\Omega$ load, internal clock)

Phase Noise:  $< -140$  dBc, 10 kHz offset, 10 MHz out.  
Spurious:  $< -70$  dBc below 10 MHz (450 MHz span)  
 $< -65$  dBc below 50 MHz  
 $< -50$  dBc below 150 MHz  
 $< -40$  dBc below 350 MHz  
Harmonic:  $< -65$  dBc below 1 MHz  
 $< -60$  dBc below 10 MHz  
 $< -50$  dBc below 25 MHz  
 $< -40$  dBc below 50 MHz  
 $< -35$  dBc below 150 MHz  
 $< -25$  dBc below 350 MHz

#### POWER REQUIREMENTS

+4.75 to +5.25 V @  $< 750$ mA. 2.5 mm center-positive connector on rear panel. AC line (100-240 V, 50-60 Hz) adapter provided.

#### SIZE

39 mm H, 107 mm W, 172 mm L, not including connectors.

#### CONNECTORS

BNCs for SINE Out, LVCMOS Out, LVDS out, EXT CLK In. SMA for external step. 2.5 mm center-positive for power. DE-9 for serial.

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**Table 2: Serial Commands**

Serial Command	Function
F0 xxx.xxxxxxxxxxxxx	Set Frequency of output in MHz to nearest 10 $\mu$ Hz. Decimal point required.
P0 N	Set Phase of output. N is an integer from 0 to 16383 (14-bits). Phase is set to $N*360^{\circ}/16384$ or $N*2\pi/16384$ radians. Sets the relative phase of the frequency output.
E x	Serial echo control. x=D for Echo <b>D</b> isable, x=E for Echo <b>E</b> nable
C x	Select clock source. x=E for <b>E</b> xternal clock of 10.0 MHz, x=I for <b>I</b> nternal Clock. When locked to 10.0 MHz the output frequency and step size must be scaled. See manual for details.
R	Reset. This command resets the 425A. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
A x	x=E for LVC <b>M</b> OS <b>E</b> nable, x=D for LVC <b>M</b> OS <b>D</b> isable.
D0 N	Set Divider value on LVC <b>M</b> OS output. N is an integer from 0 to 65535. The output frequency set by the "F0" command is divided by N+1 before being sent to the LVC <b>M</b> OS driver. ( $1 \leq$ overall divide value $\leq$ 65536). The divider value is automatically applied to the LVC <b>M</b> OS independent of the state of the "I x" command.
Pr x	x=E for Enable Prescaler, x=D for Disable Prescaler. When enabled, the frequency set by the "F0" command is divided by 2 before entering the LVC <b>M</b> OS divider specified by the "D0" command. This allows a maximum overall integer divide of 131072.
S	Saves current state into EEPROM and sets valid flag. The saved state is used as default upon next power up or reset. Use the "CLR" command to return to default values.
QUE	Return present frequency, phase and status. Returns a character string representing the hexadecimal value of internal registers.
V0 N	Set voltage level of output. In default, the amplitude is set to the maximum: approximately 0.5 $V_{rms}$ (+7 dBm) into 50 $\Omega$ . N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1024. If $N \geq 1024$ , the scaling is turned off and the output is set to full scale.
I x	Set the I/O update pulse method. If x=a, then an I/O update is issued <b>auto</b> matically at the end of each serial command (default). If x=m, then a <b>man</b> ual I/O update pulse is expected to be sent by a subsequent 'I p' command or an external control line.
<b>B</b> aabb[cc[dd[ee[ff[gg[. . ]]]]]]]]	This <b>B</b> yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the instruction word "aabb". Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than for correct format, is performed. See manual for details.