NOVATECH INSTRUMENTS, INC.

171MHz Two Frequency Signal Generator

Model 409B/02

The 409B/02 is a 171 MHz Two Channel Direct Digital Synthesized Signal Generator in a small table top case. The 409B generates four output signals simultaneously up to 171 MHz in 0.1 Hz steps under RS232 control. Each frequency has two outputs: one sine wave and one LVCMOS on adjacent BNC front panel connectors. The RS232 interface uses simple text commands to control the module and allows non-volatile storage of all settings. The 409B/02 is equipped with a ±1.5ppm on-board VCTCXO clock and can accept a rear panel external clock source up to 500 MHz.

Specifications:

OUTPUTS

TYPES: Two Sine and two LVCMOS simultaneously (LVCMOS paired with adjacent SIne). Outputs are phase-synchronous.
IMPEDANCE: Sine: 50Ω; LVCMOS: 50Ω.
RANGE: 0.1Hz to 171MHz in 0.1 Hz steps (Sine out, int. clock).
SINE AMPLITUDE: approximately $1V_{pp}$ (+4dBm) into 50Ω. Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits), or by scale factors of 1/2, 1/4, or 1/8.
PHASE: Each channel 14-bits programmable.
FLATNESS: ±3dB from 1kHz to 150MHz referenced to amplitude at 35MHz, full scale.
SINE: Output on BNCs 0 and 2. Corresponding LVCMOS are on BNCs 1 and 3. (See page 3)

LVCMOS AMPLITUDE (consult factory for availability)

V_{oh} >=2.4V and V_{ol} <=0.4V when series terminated. Rise and fall times <1.5ns with <15pF load. (specified: >1MHz, <125MHz)

CONTROL

All output frequencies (32-bits), amplitudes (10-bits) and phases (14-bits) are independently controlled by an RS232 serial port at 19.2kbaud. All settings can be saved in non-volatile memory.

ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±1ppm per year, 18 to 28°C. (Internal Clock)

EXTERNAL CLOCK IN

LEVEL: 0.2 to 0.5Vrms Sine or Square Wave. 50Ω.
FREQUENCY: 10MHz to 125MHz with PLL clock multiplier of 4 to 20 enabled. Direct input of 1MHz to 500MHz. Additional low pass filtering might be required depending upon application.

SPECTRAL PURITY (Typ. 50Ω load, internal clock, full-scale output)

Phase Noise: <-120dBc, 10kHz offset, 5MHz out.
Spurious: <-60dBc below 10MHz (typ. 300MHz span)
<-60dBc below 40MHz
<-55dBc below 80MHz
<-50dBc below 160MHz
Harmonic: <-65dBc below 1MHz
<-55dBc below 20MHz
<-45dBc below 80MHz
<-35dBc below 160MHz
(channel-channel isolation: <-60dBc)

POWER REQUIREMENTS

+4.75 to +5.25V@<750mA. AC-adapter provided.

SIZE

39mm H, 107mm W, 172mm L, not including connectors.

CONNECTORS

BNC for Outputs and EXT CLK IN. 2.5mm center positive for +5VDC power. DE9 for Serial Control.

RELATED MODELS

Model 409B-AC has four different frequencies and adds two rear-panel SMA connectors for external control of output update and table timing (see AN002). The Model 409B has four frequencies and deletes the rear panel control.

21-Dec-2009

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Table 2: RS232 Serial Commands, 409B/02

RS232 Command	Function
`Fn xxx.xxxxxxx`	Set Frequency of output "n" in MHz to nearest 0.1Hz. Decimal point required. Set to 0.00 to turn off a channel. n=2, 3. Maximum setting: 171.1276031MHz. Single tone mode.
`Pn N`	Set Phase. N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*π/8192 radians. Sets the relative phase of the frequency output depending upon the value of n=2, 3. Single tone mode.
`E x`	Serial echo control. x=D for Echo **D**isable, x=E for Echo **E**nable
`C x`	Select clock source. x=E for **E**xternal clock, x=I for **I**nternal Clock. May require adjustment of Kp and external filtering of output.
`R`	Reset. This command resets the 409B. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
`CLR`	Clear. This command clears the EEPROM valid flag and restores all factory default values.
`A x`	x=E for LVCMOS **E**nable, x=D for LVCMOS **D**isable. The LVCMOS is at the same frequency as the corresponding Sine Wave output (specified for >=1 MHz). Defaults to Disable.
`S`	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the `"CLR"` command to return to default values.
`QUE`	Return present frequency, phase and status. Returns a character string of all internal settings. Only the values relating to channels 2 and 3 have meaning for the 409B/02.
`M N`	Mode command. Mode '0' is single tone on all channels (default). This is the only mode available on the 409B/02.
`Vn N`	Set voltage level of output. In default, the amplitude is set to the maximum: approximately 1V_{pp} (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1023. n=2, 3 to set the amplitude on frequency 2 or 3. If N >=1024, the scaling is turned off and the selected output is set to full scale.
`Vs N`	Set the output scaling factor. N=1 for full scale, N=2 for one half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
`Kp aa`	Set PLL reference multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01_h, 04_h to 14_h). Values of Kp times clock frequency must not be between 160MHz and 255MHz (for internal clock, this disallows 5<=Kp<= 9).
`I x`	Set the I/O update pulse method. If x=a, then an I/O update is issued at the end of each serial command (default). If x=m, then a manual I/O update pulse is sent by a subsequent `'I p'` command.
`B aa[bb[cc[dd[ee[ff[gg]]]]]]`	This **B**yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the function. Please consult the manual for details. Note that it is possible to set the DDS chip into a non-function mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed.

409B/02 Front View