NOVATECH
INSTRUMENTS, INC.

100MHz Quadrature Signal Generator

Model 408A

The 408A is a 100MHz Direct Digital Synthesized Signal Generator in a small table-top shielded enclosure. The 408A generates Sine/Cosine and ACMOS/TTL output signals simultaneously up to 100MHz in 1µHz steps under serial control. The RS232 interface uses simple text commands to control the module and allows non-volatile storage of all settings. The 408A is equipped with a ±2ppm VCTCXO clock or it can be set to accept an external clock source up to 300MHz. Up to four Model 408A can be mounted in a single 1U rack using the optional rack adapter. The 408A operates from +5VDC supplied by a provided AC-line adapter. SOF8 host software included.

Specifications:

OUTPUTS
TYPES: Sine, Cosine and ACMOS/TTL simultaneously.
IMPEDANCE: 50Ω.
RANGE: 100Hz to 100MHz in 1µHz steps (int. clock).
SINE/COS AMPLITUDE: approximately +7dBm (0.5Vrms) into 50Ω load. Programmable from 0/4096 to 4095/4096 of Full Scale (12 bits internal control).
FLATNESS: ±3dB from 10kHz to 100MHz referenced to amplitude at 30MHz, stable to <±1dB from 18-28^{o}C.

ACMOS/TTL AMPLITUDE
V_{OL}<0.5V, V_{OH}>2.5V into a 15pF load. $T_{r,f}$ <5ns. Duty Factor: 45-55%. 50Ω.

CONTROL
Output frequencies, phase (14 bits) and modes are controlled by an RS232 serial port at 19.2kbaud. All serial settings can be saved in non-volatile memory. (some modes require external parallel connection: consult factory)

ACCURACY AND STABILITY
Accuracy: <±2ppm at 10-40^{o}C. Stable to an additional ±3ppm per year, 18-28^{o}C. (Internal Clock)

EXTERNAL CLOCK IN
LEVEL: 0.35-2.5Vrms Sine or Square Wave. 50Ω.
FREQUENCY: 5MHz to 75MHz. Multiplier of 4x to 20x selected via control port (may be bypassed for up to 300MHz direct input). Output may require additional filtering for optimum performance when external clock is used. Clock source selected by internal jumper.

SPECTRAL PURITY (Typ. 50Ω load, internal clock)
Phase Noise: <-140dBc, 10kHz offset, 5MHz out.
Spurious: <-70dBc below 10MHz (typ. 200MHz span)
<-65dBc below 40MHz
<-50dBc below 100MHz
Harmonic: <-65dBc below 1MHz
<-60dBc below 10MHz
<-50dBc below 20MHz
<-40dBc below 50MHz
<-35dBc below 100MHz

SWITCHING TIME
RS232 control depends upon host speed and commands sent, typ. <10ms for a new frequency.

POWER REQUIREMENTS
+5Vdc, (+4.5 to +5.5Vdc) <1.0 Amp, AC line (100 to 240VAC) to DC adapter provided. Reverse voltage and over-current protected.

SIZE
39mm H, 107mm W, 172mm L, not including connectors.

CONNECTORS
Front panel BNCs for Cosine (I), Sine (Q) and Clock Out. Rear panel BNC for EXT CLK IN and rear panel DE9 for RS232. Rear panel 2.5mm power receptacle for +5V IN, center positive.

13-Apr-2006

NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America
http://www.novatech-instr.com/
novatech@eskimo.com
206.363.4367 FAX/206.301.8986 Voice

RS232 Command	Function
F0 XX.XXXXXXXXXXX	Set Frequency in MHz to nearest 1µHz. Decimal point required.
F1 XX.XXXXXXXXXXX	Start Frequency in MHz to nearest 1µHz. Decimal point required. Same as F0 if Mode 0 is selected.
F2 XX.XXXXXXXXXXX	Stop Frequency in MHz to nearest 1µHz. Decimal point required. Modes 1 and 2.
Fd XX.XXXXXXXXXXX	Delta Frequency in MHz. Software sets to nearest 1µHz. Decimal point required.
E x	x=D for Echo **D**isable, x=E for Echo **E**nable
Q x	x=D for Q-channel **D**isable, x=E for Q-channel **E**nable
R	Reset. This command resets the 408A. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
Px N	Set Phase. N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*π/8192 radians. Sets either the phase P1 or P2 depending upon the value of x (1 or 2). The I and Q outputs are always nominally 90^{o}. In Mode 0, this sets the static phase. In Mode 4, the phase is either P1or P2 depending upon the state of Pin 8 of the parallel connector.
A x	x=E for ACMOS/TTL **E**nable, x=D for ACMOS/TTL **D**isable
S	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the "CLR" command to return to default values.
QUE	Return present frequency, phase and status. Returns an 80-character string of all internal settings: hexadecimal format. See Table 7.
M N	Mode command. N is 0, 1, 2, 3 or 4. 0 is Single Tone, 1 is FSK (pin 8 of parallel port is active), 2 is Triangular Ramped Frequency, 3 is Chirp Frequency and 4 is BPSK (pin 8 is active). Defaults to Mode 0 upon turn-on, unless another mode is saved. Some modes require external connections. See Appendix A of the DDS8m manual.
Td N	Time at each Fd (see Appendix A). N is an integer from 0 to a maximum value of 2^{20}-1 or 1048575. Applies to modes 2 and 3 only. Approximately 3.5ns increments using internal clock. In mode 2, frequency ramps from F1 to F2 and returns to F1 continuously in steps of Fd at time intervals of Td.
Tr N	Repeat time in mode 2 and 3. In mode 3, the frequency will ramp starting at F1 in steps of Fd, at time intervals Td, until Tr times out, repeating continuously from F1. N is an integer between 5 and 2^{32}-1 (4294967295). Approximately 7.0ns increments with the internal clock. A 3.3V CMOS level pulse at the start of each ramp is provided on Pin 10 of the parallel I/O connector. Approximately 40ns (8 system clocks) wide for the internal clock. In Mode 2, Tr sets the timing of an external trigger pulse on Pin 10 of the parallel interface.
Vx N	Set voltage level of output. In default, the amplitude is set to the maximum: approximately +7dBm into 50Ω. N can range from 0 (off) to 4095 (no decimal point allowed). Voltage level is scaled to N/4096. x is I or Q to set the amplitude on the I or Q channel. If N >4095, the scaling is turned off and both outputs are set to maximum. Overrides the "Z" command.
Kp aa	Set PLL reference multiplier constant. Must be one Hex byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01_h, 04_h to 14_h).
Z N	Turns on 30% Amplitude Modulation of Cosine (I) channel output. N is the frequency of modulation in 100Hz steps, 900Hz maximum (9). N = 0 turns off modulation. Use of this command overrides the V command on the I channel. Entering any "M" command turns off modulation.
B aadd	Set a data byte "dd" at address "aa" in Hex. Allows setting of all internal registers. "aa" is in the range of 00_h to 27_h while "dd" is from 00_h to ff_h. No error checking, other then correct format, is performed. It is possible to set the 408A into a nonfunctional state requiring a power cycle to recover with this command.