

# MODEL 1450A/02-AH Synthesizer

## **NOTE:**

*This is a preliminary manual for the Novatech Instruments, Inc. Model 1450A/02-AH Synthesizer.*

## **WARNING:**

*Live line voltages are exposed internal to the instrument. Do not operate with covers removed. Disconnect power cord before opening instrument for any reason.*

## **Specifications:**

**OUTPUTS:** There are up to nine DDS8p synthesizers internal to the 1450A/02-AH. The output frequency range of each is 10kHz to 120MHz, AC MOS, in 1 $\mu$ Hz steps per LSB on the parallel interface. Outputs are SMA female on rear panel, 50 $\Omega$ . See below for operating modes.

**INPUT:** External Clock, 10MHz  $\pm$ 5ppm, >1Vrms, 50 $\Omega$ . Circuitry detects, locks to and tracks this input when present. An internal TCXO (10MHz  $\pm$ 2ppm) is used if the 10MHz external clock input is left unconnected. SMA Female.

**PHASE and FREQUENCY CONTROL:** The Parallel interface is on a 90-pin EDAC 516-series connector receptacle on the rear panel. An adapter board for use with ribbon cables is available. See below for connector details.

**SIZE:** 19inch 2U rackmount case with mounting ears, 16inches deep, not including connectors.

**POWER:** 120/240VAC, 50/60Hz, <75VA.

**ENVIRONMENTAL:** Intended for laboratory/central office environment of: +5 $^{\circ}$ C to +40 $^{\circ}$ C with humidity 80% to 31 $^{\circ}$ C, decreasing linearly to 50% at 40 $^{\circ}$ C.

**OPERATION:** Illuminated front panel power switch. Rear panel mode select switch. Front panel "IN LOCK" and "POWER OK" LEDs.

## **Installation Notes:**

The 1450A/02-AH contains up to nine independent synthesizers addressable through the various control signals on the parallel interface connector.

See signal description, timing diagram, timing table and signal notes below for operation.

### REAR PANEL CONTROL receptacle

EDAC PIN	Function	EDAC PIN	Function	EDAC PIN	Function
A	Frequency Bit0 (FB0) (LSB)	AK	FB30	BU	PB12
B	FB1	AL	FB31	BV	PB13 (MSB)
C	FB2	AM	FB32	BW	RESERVED
D	FB3	AN	FB33	BX	RESERVED
E	FB4	AP	FB34	BY	RESERVED
F	FB5	AR	FB35	BZ	RESERVED
H	FB6	AS	FB36	CA	RESERVED
J	FB7	AT	FB37	CB	RESERVED
K	FB8	AU	FB38	CC	RESERVED
L	FB9	AV	FB39	CD	RESERVED
M	FB10	AW	FB40	CE	RESERVED
N	FB11	AX	FB41	CF	RESERVED
P	FB12	AY	FB42	CH	RESERVED
R	FB13	AZ	FB43	CJ	RESERVED
S	FB14	BA	FB44	CK	RESERVED
T	FB15	BB	FB45	CL	RESERVED (RAC)
U	FB16	BC	FB46	CM	RESERVED (PFR)
V	FB17	BD	FB47 (MSB)	CN	Phase/Freq Strobe0 (PF0)
W	FB18	BE	Phase Bit0 (PB0) (LSB)	CP	PF1
X	FB19	BF	PB1	CR	PF2
Y	FB20	BH	PB2	CS	PF3
Z	FB21	BJ	PB3	CT	PF4
AA	FB22	BK	PB4	CU	PF5
AB	FB23	BL	PB5	CV	PF6
AC	FB24	BM	PB6	CW	PF7
AD	FB25	BN	PB7	CX	RESERVED (MODE)

**REAR PANEL CONTROL receptacle**

EDAC PIN	Function	EDAC PIN	Function	EDAC PIN	Function
AE	FB26	BP	PB8	CY	MR- (Factory)
AF	FB27	BR	PB9	CZ	Common Freq. Strobe (CFS)
AH	FB28	BS	PB10	DA	BUSY
AJ	FB29	BT	PB11	DB	Signal Ground (SG)

**Parallel Input Requirements****NOTE:**

*The control inputs are protected against ESD damage by 100Ω series termination resistors (typically ±2kV, Human Body Model. ±200V, machine model).*

*The inputs on the 1450A/02-AH are 3.3V and 5.0V CMOS logic tolerant.*

**NOTE:**

*The connector used on the rear panel is an EDAC 516-090-520-302 receptacle.*

All of the inputs, **FB0-47**, **PB0-13**, **PF0-7**, **CFS** and **MR-**, are VHCMOS, TTL and 5V CMOS compatible and require:

$$V_{il} \leq 0.8V \quad (I_{load} < -1.0mA)$$

$$V_{ih} \geq 2.4V \quad (I_{load} < 1.0mA)$$

$C_{in}$  on each pin is approximately 15pF (application cable capacitance not included). All the input pins are pulled to the +5V internal  $V_{CC}$  via pull-up resistors (approximately 4.7kΩ). They are series terminated with a resistance of 100Ω to prevent reflections and ringing. You may need to supply source termination resistors for your control signals, depending upon your cabling. The exact value will be determined by your application.

Reserved pins must be left unconnected, except as noted here. Three control pins are available: RAC, PFR and MODE. RAC is used to **Reset AC**cumulators in the internal synthesizers and is used during factory test. PFR operates exactly like all the PF<sub>n</sub> lines, except it controls the reference synthesizer. This allows each of the nine synthesizers to be used independently if desired. MODE can be used to select Synchronous or Independent mode without using the switch. If used, it overrides the switch. Normally left unconnected. (the rear panel switch must be left in the SYNC position if the MODE line is used).

**Signal Descriptions (INDEPENDENT MODE):**

The Independent Mode allows each of the internal eight (nine, if PFR is used) synthesizers to be used

at independent frequencies and timing. Phase is not controlled in this mode.

**FB0** through **FB47** are the 48 binary frequency data bits presented to the internal DDS. The frequency output will have 1 $\mu$ Hz of resolution per LSB. Since there is no error checking of the user input, care must be taken ensure that the binary value does not select a frequency output greater than approximately 120MHz.

**PB0** through **PB13**. Since the frequency and operation of each synthesizer is independent in this mode, the Phase value on the lines PB0 through PB13 are “*don't care*.” It is suggested that they be held LOW in this mode.

Any **PF0-7** going LOW is used to signal the on-board circuitry to load a new frequency into the corresponding DDS registers. The negative edge of PF is latched, inverted and presented on the BUSY line. The negative edge also transfers data from the user application connection to internal latches. Data must be stable at least 25ns before the negative edge of PF. During BUSY, all appropriate registers on the selected internal DDS8p are programmed and upon completion of the loading process a new frequency is available at the output. The on-board circuitry takes approximately 170ns to set the new frequency after BUSY has returned LOW. The timing of BUSY returning LOW may have several internal clock cycles of ambiguity due to timing re-synchronization internal to the parallel interface board ( $\pm 200$ ns). Each separate output is set on PF0-7 going low. The other unselected synthesizer outputs remain unchanged.

**NOTE:**

*The delay DDS outputs on the rear of the 1450A/02-AH are numbered beginning with “1.” PF0 controls output #1, while PF1 controls output #2 and so on. The Reference DDS is controlled by PFR.*

**BUSY** is a VHCMOS compatible *output* with:

$$V_{oh} \geq 3.0 \text{ V } (I_{load} \leq -100\mu\text{A})$$

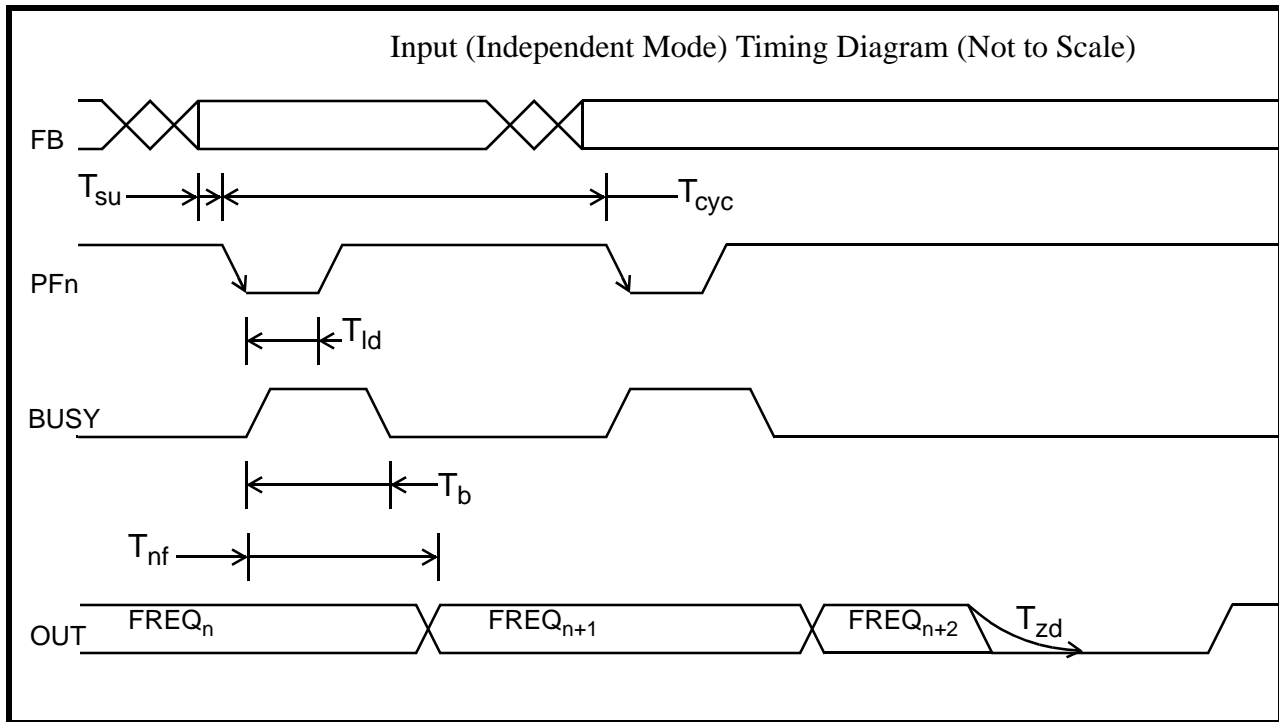
$$V_{ol} \leq 0.4\text{V } (I_{load} \leq 100\mu\text{A})$$

**BUSY** going HIGH indicates that parallel data is being loaded into the DDS circuitry. The output frequency is updated approximately 170ns *after* BUSY returns LOW. Please refer to timing diagram for details.

**BUSY** has a source resistance of approximately 100 $\Omega$  to prevent damage due to accidental shorts. If this output is used for handshaking, be sure to account for capacitive loading on this signal.

**CFS** is not used in this mode and must be held HIGH, or left open (internal pull-up).

Please refer to the timing diagram and table below for the details of setting frequency on the parallel interface in the independent mode.

**Table 1: Timing, Independent Mode.**

Parameter	Name	Min	Max	Notes
$T_{su}$	Binary Data Setup	25ns		Binary Data Stable before PFn.
$T_{ld}$	PF Pulse Width Low	100ns		Minimum PF pulse width.
$T_b$	Busy Time		430ns	BUSY is HIGH for internal data transfer.
$T_{nf}$	New Frequency Time		600ns	New frequency on output.
$T_{zd}$	Zero Decay Time		10 $\mu$ s TYP	Time for Output to decay to $\pm 100$ mV after setting frequency to zero (Sine output only). Square wave output may be erratic during this time.
$T_d$	Busy LOW to output		170ns	Time for new output to stabilize after BUSY returns LOW.
$T_{cyc}$	Load cycle time	600ns TYP		Cycle time before next PF.

**MR-** is the master reset signal (guaranteed for Factory Use Only). When LOW all the circuitry internal to the 1450A/02-AH is reset. Upon returning HIGH, the 1450A/02-AH will initialize in less than 250ms and output a frequency of 10.0MHz and 0° phase. Toggling MR- performs the same function as cycling power. An internal reset is issued upon change of the MODE switch. MR- must be low for at least 1ms.

After a power cycle, mode change or MR-, the 1450A/02-AH takes approximately 500msec to

initialize.

### **Signal Descriptions (SYNCHRONOUS MODE):**

In the synchronous mode, all internal synthesizers are set to the same frequency and programmed with phase offsets from the reference synthesizer. The reference synthesizer must always be set to  $0^\circ$  phase using the PFR control line.

#### **NOTE:**

*The 1450A/02-AH performs a reset sequence whenever the Mode is changed between Synchronous and Independent. The output will return to the default (all 10.0MHz) following a Mode change.*

**FB0** through **FB47** are the 48 binary frequency data bits presented to the internal DDS. The frequency output will have  $1\mu\text{Hz}$  of resolution per LSB. Since there is no error checking of the user's input, care must be taken to ensure that the binary value does not select a frequency output greater than approximately 120MHz. During programming of all phases, these lines must be held constant at the desired frequency setting.

**PB0** through **PB13** are the 14 binary phase data bits presented to the internal DDS. The phase of the output will change by  $N \cdot 360^\circ / 16384$  or  $N \cdot \pi / 8192$  radians, where N is the value of the binary bits. The reference synthesizer must always be set to  $N=0$ .

#### **NOTE:**

*With a resolution of 14-bits, the phase can be set to within  $0.022^\circ$ . This corresponds to approximately 6ps at 10MHz. Dispersion due to various propagation delays is greater than this and must be taken into account in the customer application.*

**PFR**, with **PB0** through **PB13** set to zero phase and **FB0** through **FB47** set to the desired frequency, must be pulsed to set the proper reference phase and frequency.

Any **PF0-7** going LOW is used to signal the on-board circuitry to load a new phase (and frequency, which must be held constant) into the corresponding DDS registers. After all phases are loaded, CFS (common frequency strobe) is pulled low to set all the outputs simultaneously. In this mode, **BUSY** is not asserted until CFS goes active (see below). To program the synchronous mode properly, the signals **FB0-FB47** must be held constant for all **PFn**. Only the relative phases should be changed. While each assertion of a **PFn** line causes a load sequence taking approximately 430ns on each internal synthesizer, new data can be set up for the next **PFn** following a T1d period. CFS must not be asserted until after **BUSY** returns to an idle state following the last phase setting.

**CFS**. The negative edge of CFS is inverted and presented on the **BUSY** line and must be asserted after all synthesizers have been loaded with appropriate phase data. The last **BUSY** from any **PFn** load must be stable low at least 25ns before the negative edge of CFS. The on-board circuitry takes approximately 170ns to set the new frequency after CFS has pulsed LOW. For each synthesizer to have the same frequency, **FB0-47** must be held constant at the desired frequency during all **PFR** and **PF0-7** cycles.

**BUSY** is a VHCMOS compatible *output* with:

$$V_{oh} \geq 3.0 \text{ V } (I_{load} \leq -100\mu\text{A})$$

$$V_{ol} \leq 0.4\text{V } (I_{load} \leq 100\mu\text{A})$$

**BUSY** going HIGH indicates that all parallel data is being loaded into the DDS circuitry and the new frequency is unstable. The output frequency is updated approximately 170ns *after* the BUSY caused by CFS pulses HIGH. The length of CFS LOW is not critical. Please refer to timing diagram for details.

**BUSY** has a source resistance of approximately 100Ω to prevent damage due to accidental shorts. If this output is used for handshaking, be sure to account for capacitive loading on this signal.

Please refer to the timing diagram and table below for the details of setting frequency and phase on the parallel interface in the synchronous mode.

**MR-** is the master reset signal. When LOW all the circuitry internal to the 1450A/02-AH is reset. Upon returning HIGH, the 1450A/02-AH will initialize in approximately 250ms with an output frequency of 10.0MHz and 0° phase. Toggling MR- performs the same function as cycling power. A reset is issued upon change of the MODE switch. MR- must be low for at least 1ms.

After a power cycle, mode change or MR-, the 1450A/02-AH takes approximately 250msec to initialize.

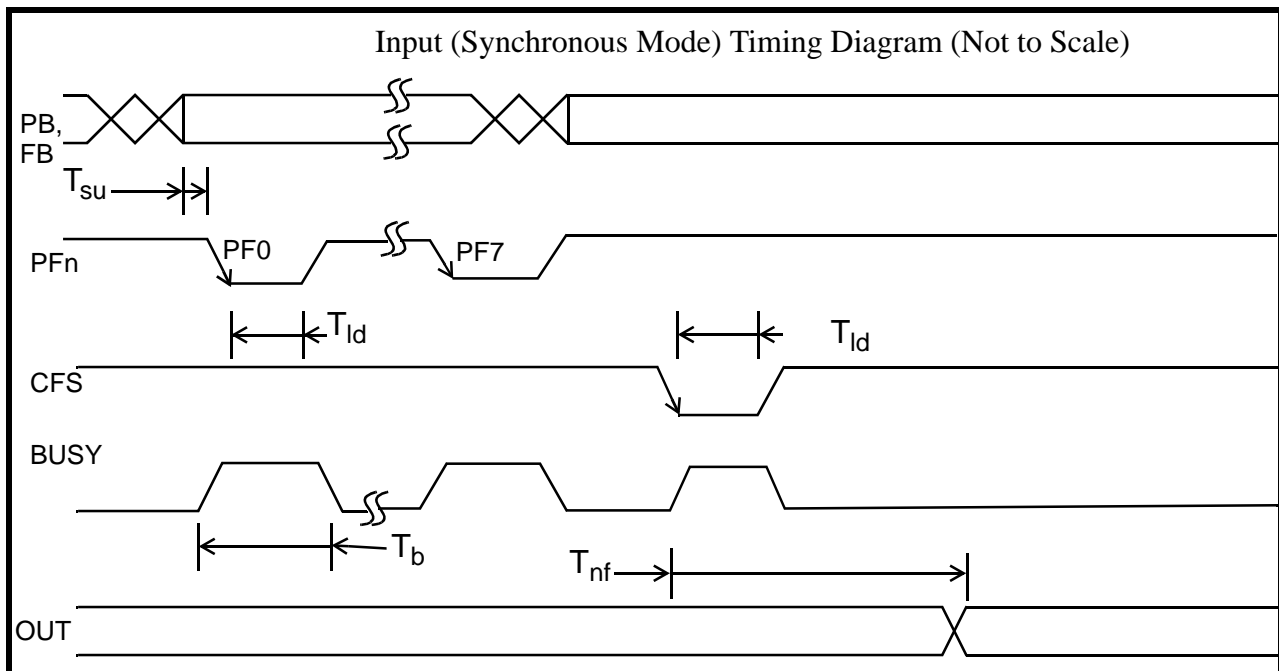


Table 2: Timing, Synchronous Mode.

Parameter	Name	Min	Max	Notes
$T_{su}$	Binary Data Setup	25ns		Binary Data Stable before PFn or CFS.
$T_{ld}$	CFS or PF Pulse Width Low	100ns		Minimum CFS or PF pulse width.
$T_b$	Busy Time		1.3 $\mu$ s	BUSY is HIGH for internal data transfer.
$T_{nf}$	New Frequency Time		200ns	New frequency and phase on output.
$T_{cyc}$	Load cycle time	2.5 $\mu$ s TYP		Cycle time before next CFS time.
$T_{disp}$	Delay Dispersion	-10ns	+10ns	Zero Phase Delay with respect to reference synthesizer.

### **Operational Notes:**

Upon power up or changing of the clock source, the internal clock generator may take up to one minute to lock to within 0.1ppm of the 10MHz internal master clock or the external 10MHz. The external clock must be 10MHz  $\pm$ 5ppm and  $>1V_{rms}$  into the 50 $\Omega$  input impedance (square wave or sine wave). A MR- restarts this timing period. The phase between the external clock input and any of the synthesizer outputs is not controlled. During out-of-lock or during a lock acquisition time, the front panel "LOCK" LED will be dark.

Delay Dispersion. Due to various propagation delays and anti-alias filter group delays, outputs set to zero phase (delay) in the synchronous mode may be offset from the reference synthesizer  $\pm$ 10ns. The 14-bit resolution of the phase control allows this to be accounted for and calibrated out by the user application. This dispersion will vary with frequency. Note that equal lengths of ordinary coaxial cable will have dispersion characteristics much greater than the resolution of the phase (delay) control and this must be taken into account in the final application.

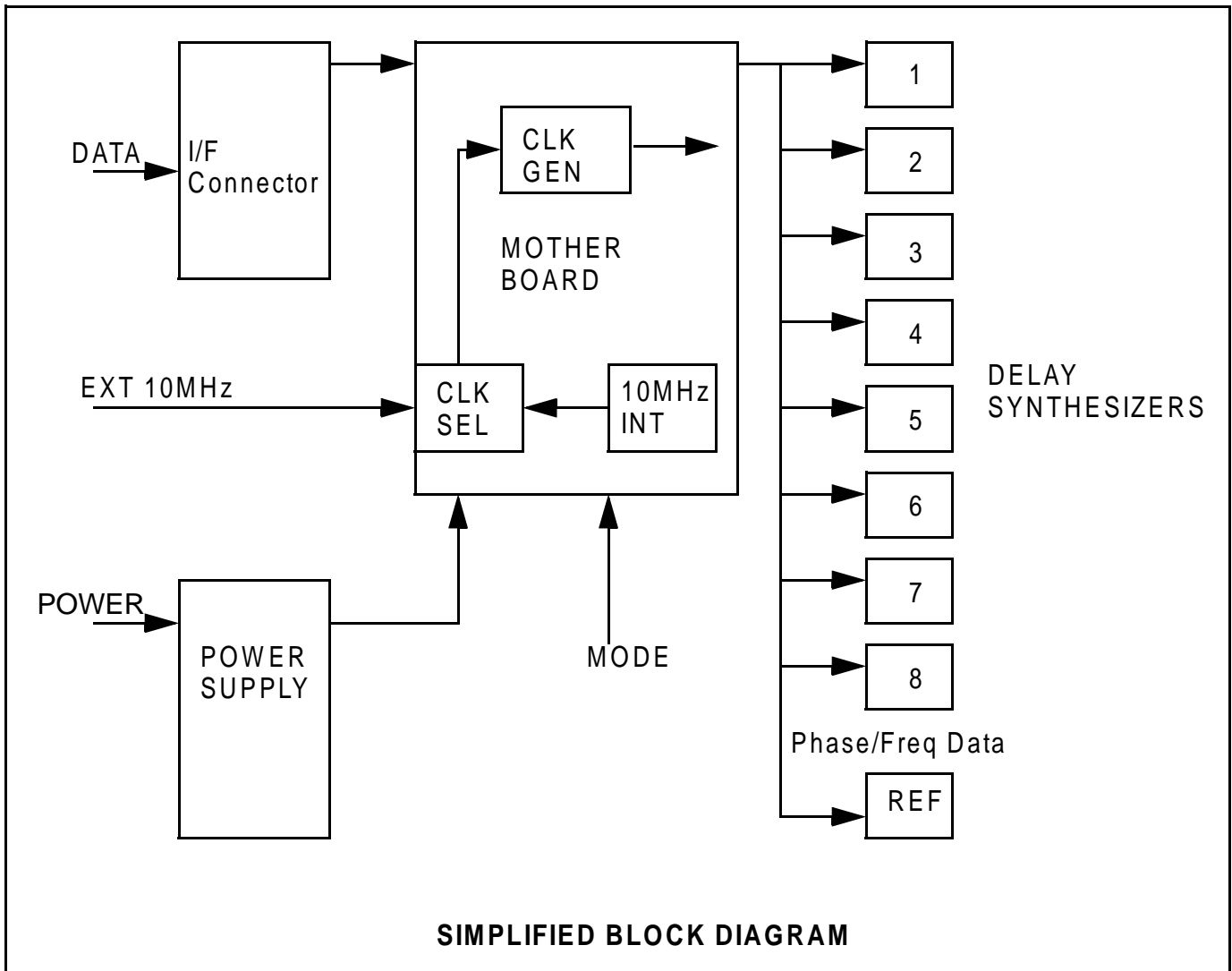
Changing the MODE via the control pin on the connector or by the rear panel switch will initiate a MR- cycle. This ensures that all synthesizers are properly initialized.

### **Mechanical Notes:**



The Model 1450A/02-AH is housed in a 19-inch, 2U rack, 18-inches deep. The rear panel photo is





shown above. Note that Pin “A” of the EDAC interface connector is in the upper left corner of the connector. The connector, without pins inserted, is shown below:



## WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

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