AN-451

Application note

A FREQUENCY COUNTER USING MOTOROLA RTL INTEGRATED CIRCUITS

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A frequency-period counter with a total hardware cost under $200.00, based on unit quantity prices, is described. The instrument measures the periods and frequencies of periodic waveforms, ranging in frequency from 10 Hz to 20 MHz, and counts random occurances for selected gate times of one millisecond to 10 seconds. A four digit decimal readout is provided. The low cost is achieved by utilizing plastic MRTL devices in unique versions of a crystal controlled oscillator, a period selector, a one shot multivibrator, a pulse shaper, and a switch contact bounce eliminator circuit.

MOTOROLA *Semiconductor Products Inc.*

INTRODUCTION

With the advent of plastic encapsulated integrated circuits, especially the recent introduction of multifunction digital circuits, a price revolution has developed in the cost of complex instrumentation. Appearing on today's market are frequency counters and digital voltmeters neighboring $1500, which not long ago demanded prices four times over.

This report describes a frequency counter using the most inexpensive digital line available, plastic MRTL. From a system viewpoint or a block diagram analysis, nothing new is presented. However, several circuits employ the use of the MRTL gate in unique applications such as a one shot multivibrator, with a range of nanoseconds to seconds; a period selector, which allows only a single period duration to pass; a crystal controlled oscillator which is accurate and stable to within ±0.01% over the MRTL device temperature range of +15°C to +55°C, and a switch contact bounce eliminator. An MRTL hex inverter is used in a Schmitt trigger configuration. Complete specifications for the counter are listed in Table 1.

SYSTEM DISCUSSION

The functional blocks of the system are shown in Figure 1. In the frequency mode of operation, the incoming signal is amplified or limited, as warranted. It is then conditioned by the pulse shaper in order to meet the constraints imposed by the MRTL devices. The resulting pulse train, whose frequency is directly dependent on the incoming frequency, is one of the inputs of the count gate.

The 1 megahertz oscillator signal is appropriately divided down, depending on the position of the frequency multiplier switch, and routed through the period selector to the second input of the count gate. This results in turning the count gate on for a specific "gate time". The output of the count gate is then a burst of pulses, the number of which is directly proportional to the original input frequency. These pulses are then counted by the decade counting units (DCU's), each of which contains a BCD decade counter, BCD to decimal converter and produces one digit of the readout. The count is retained in the readout until the system is reset.

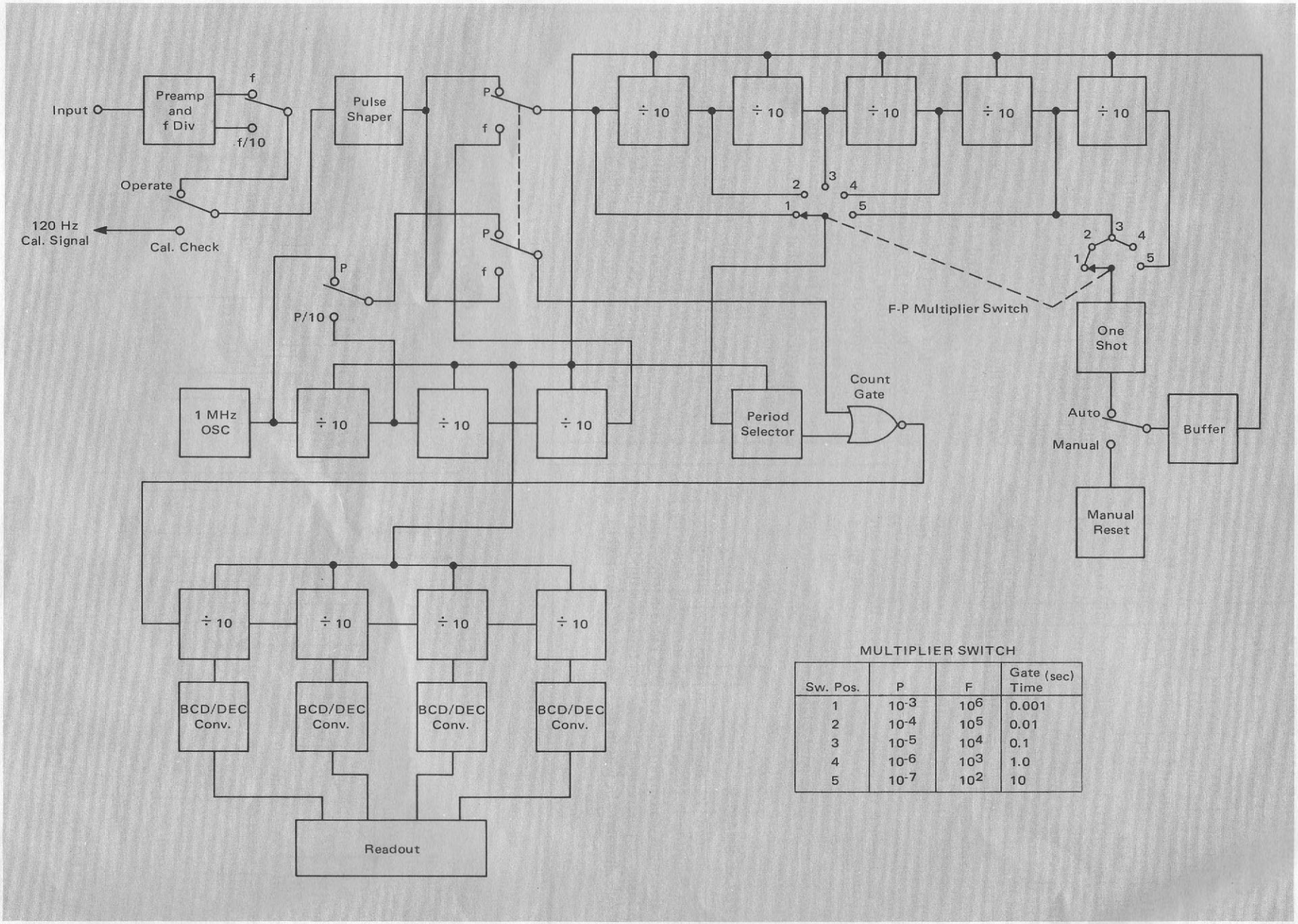
Reset is accomplished by applying a "high" or logical one to all direct clear (C_D) inputs of the flip-flops and decade counters. In the manual reset mode, this is done by a momentary push button switch. In the automatic reset mode, and in all but the number 5 multiplier switch position the output of the decade divider seven removed from the oscillator is used to do the resetting. This particular output goes high during the 8th and 9th second from zero time (that time immediately following the previous reset cycle). Once this high signal is applied to the C_D inputs, the devices are reset, therefore they are effectively reset at the beginning of the 8th second. In the number 5 multiplier switch position, since the gate time is 10 seconds, it is necessary to take the auto reset signal at the Q3 output of the 8th decade divider and reset occurs at the 40 second point. Since it is necessary to hold each C_D high for a minimum of 100 nanoseconds to insure resetting of all flip-flops, a one shot multivibrator is used. The signal triggers the one shot, which holds the reset signal high for approximately 5 microseconds. The 5 microsecond value is strictly arbitrary, however, consideration should be given to various propagation delays due to stray line capacitances and inductances, etc., throughout the system. The output of the one shot is buffered to provide sufficient drive for all C_D inputs.

The operation in the period mode is essentially the same with one major exception. The incoming signal is routed through the period selector and is used as the gate time of the count gate, whereas the oscillator signal is used as the events counted.

The self-contained calibration feature is obtained most inexpensively. It amounts to simply counting the frequency or period of the 120 Hertz signal. (In larger cities the frequency accuracy of the 60 Hertz power line is normally within ±0.05 Hertz or 0.083%.) This "line calibration" will guarantee an accuracy of ±0.1%, which will verify that the counter is at least functioning to the indicated accuracy. For more accurate calibration an external calibration signal is recommended. A calibration adjustment is provided in the oscillator section.

TABLE 1 –
Complete Specifications of MRTL Frequency/Period Counter

Waveforms measured:	sine; square; or negative pulses with greater than 30 ns duration.
Type of measurement:	frequency; period; random pulse counting with selected gate times.
Input impedance:	10 kΩ typical, 7 kΩ minimum (AC Z_{in} in the sensitive voltage range is dependent on the forward conductance of the input protection diodes, and diminishes rapidly under over-driven conditions.)
Input frequency range:	10 Hz - 20 MHz guaranteed 4 Hz - 30 MHz typical
Input period range:	50 nanoseconds to 100 milliseconds
Gate time selection:	1 millisecond to 10 seconds in decade steps.
Input protection:	±50 Vdc; 1 Volt Peak in the unattenuated position; conservatively up to 200 volts peak in the attenuated position.
Input sensitivity:	50 mv rms guaranteed, 25 mv rms typical.
Readout:	4 digit decimal; fixed decimal point location; ranging accomplished by rotary switch.
Accuracy:	±0.05% ±1 count, with self-calibration using line frequency, to ±0.1%.
Resetting:	Manual or Automatic.



MULTIPLIER SWITCH

Sw. Pos.	P	F	Gate (sec) Time
1	10^{-3}	10^{6}	0.001
2	10^{-4}	10^{5}	0.01
3	10^{-5}	10^{4}	0.1
4	10^{-6}	10^{3}	1.0
5	10^{-7}	10^{2}	10

FIGURE 1 – Block Diagram of Frequency-Period MRTL Counter.

THE PREAMPLIFIER AND PRESCALER

The preamp of Figure 2 uses a standard configuration of the MC1552G video amplifier. Two input amplitude ranges are provided, 50-300 mV rms and greater than 300 mV rms. The 3 dB down points of the preamp circuit only, in the unattenuated position as shown, are 4 Hz and 42 MHz for small signal applications. Input impedance is typically 10 kΩ.

Since the MRTL devices are guaranteed only to 4 MHz, an MDTL decade counter (MC838P) is utilized to extend the frequency range to 20 MHz.

Note that the V_{CC} of +5 volts for the decade counter is derived from the +6 volt supply by placing a silicon diode in the line. This places V_{CC} well within the supply tolerances of MDTL.

In order to attain the high frequencies specified, care must be taken in constructing the preamp. Primal is the shielding between input and output circuitry and for this reason double clad PC board was used, with the input and output components located on different sides of the board. The preamp was constructed in a separate box within the chassis. A subsequent photograph shows the location of the preamp.

THE PULSE SHAPER

As mentioned in the system discussion, the pulse shaper's function is to condition the incoming signal to meet the input constraints of the MRTL, J-K flip-flops. The primary requirement is for the fall time of a flip-flop's clock pulse inputs to be within the range of 10 ns to 100 ns. (Not applicable to the MC778P). This is accomplished by using one-half of a hex-inverter, connected in a Schmitt trigger configuration as shown in Figure 3.

The equivalent circuit is shown in Figure 4. Pin 4 of the device, the normal ground connection, is connected through the 68 ohm resistor. This resistor establishes an input hysteresis, (V_h) of 0.74 volts and also serves as the regeneration resistance. The input threshold is $V_{th} = V_h + V_{on}$ or 0.74 + 0.86 V, about 1.6 V. Under worse case conditions (15°C and 4 MHz) V_{th} is about 2 V. Inputs to the pulse shaper can be periodic waves of any form or random pulses. The one constraint is a minimum input pulse duration of 30 ns. The open circuit output voltage levels are V_{CC} for the logical "1", and $V_h + V_{CE}$ or 1.04 V for logical "0". The output rise and fall times are less than 100 ns for frequencies down to 10 Hz.

The output of the pulse shaper is diode-coupled to a buffer which provides an adequate drive capability.

Diode rather than capacitive coupling is used because of the large value of capacitance that would be required at the lower frequencies of the counter. A large capacitance would result in a very large time constant and would require an electrolytic capacitor that would become quite inductive at high frequencies.

The IN4001 diode was chosen since it functions somewhat as a capacitance at the higher frequencies due to its 50 pf, or so, of junction capacitance. At the lower frequencies it is more advantageous than a capacitor since it prohibits the signal input to the buffer from going below ground. The diode also drops the dc level by 0.7 V and insures the required V_{off} level of the MRTL buffer.

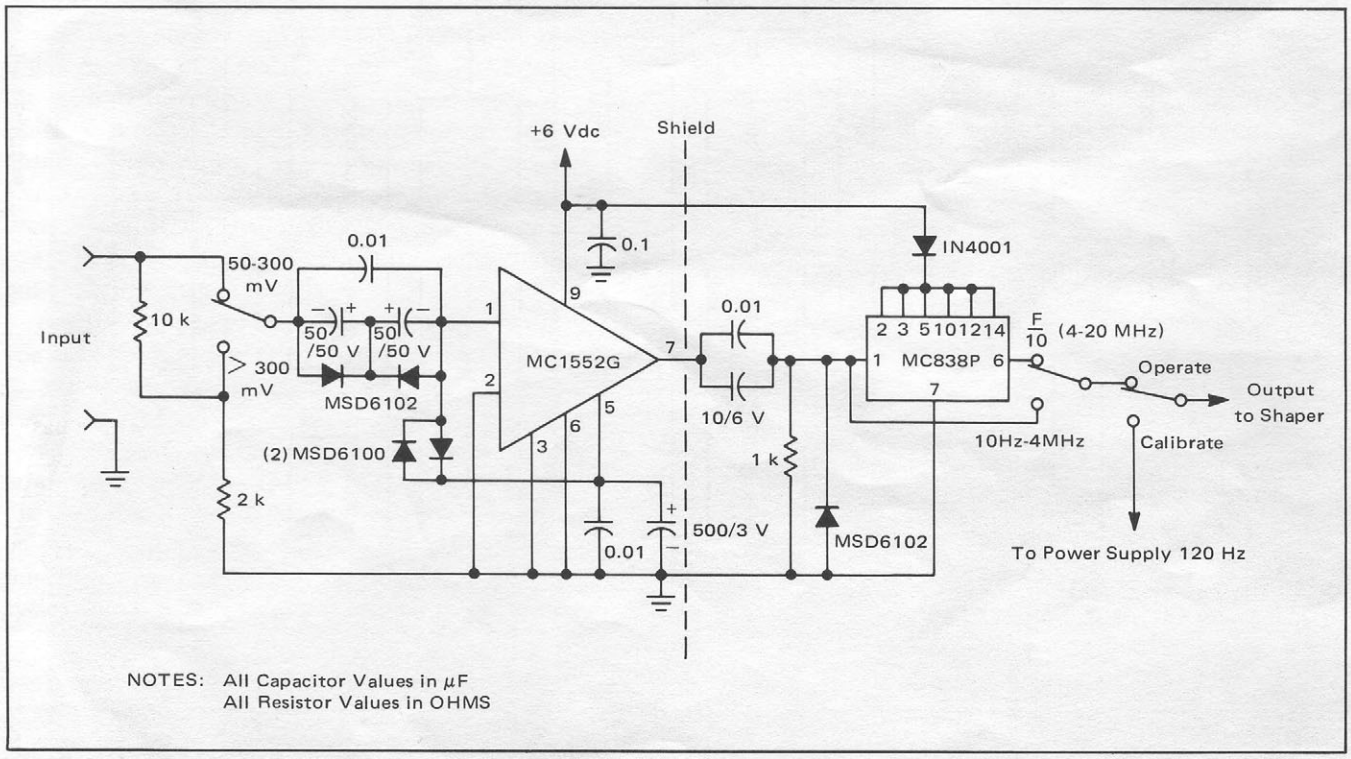


FIGURE 2 – Preamp and Prescaler.

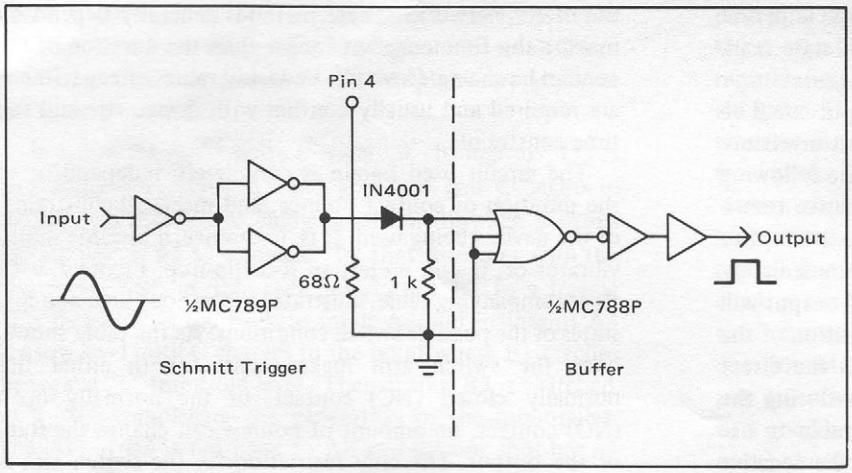


FIGURE 3 – MRTL Pulse Shaper (Schmitt Trigger with Buffered Output).

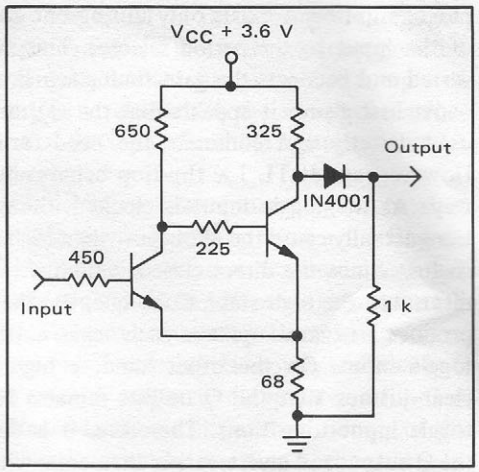


FIGURE 4 – Equivalent Circuit of Schmitt Trigger of Figure 3.

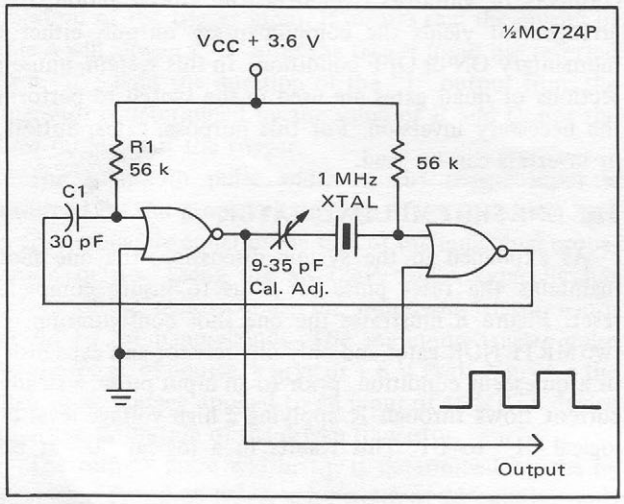


FIGURE 5 – MRTL 1 MHz Crystal Oscillator.

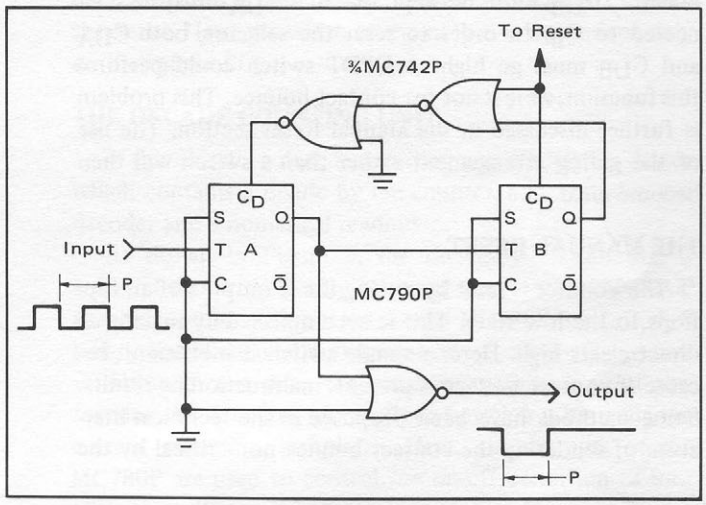


FIGURE 6 – MRTL Period Selector.

THE CRYSTAL CONTROLLED OSCILLATOR

In the oscillator of Figure 5 two gates are connected in a cross-coupled configuration, which in essence is a free-running multivibrator whose square wave output frequency is locked by the crystal. The resistors serve as biasing elements, in addition to being a part of the circuit time constants. With the crystal placed as shown, however, R1 and C1 determine the period. Since R1 also establishes the bias of the gate input, and must be fixed for a given V_{CC}, C1 and the crystal, of course, would be changed if another frequency is desired. Typical values of C1 for other frequencies are 430 pF for 500 kHz and 0.001 μF for 100 kHz.

The trimmer capacitor permits exact adjustment of the frequency, which is stable to within ±0.01% from +15°C to +55°C, without a crystal oven.

In the normal production of MRTL devices, the transistor β's will vary from about 15 to 80. This is quite acceptable for logic circuitry, but when the devices are used for an oscillator, such as described, care must be taken to select devices with sufficiently high β.

THE PERIOD SELECTOR

The function of the period selector is to accurately select one and only one period of either the incoming signal to the counter, with the counter in the period mode, or of the oscillator, with the counter in the frequency mode. The period selected, in the form of a low or logical zero, is then used as the gate time for the NOR logic count gate. In the period mode, the count gate allows passage of the oscillator signal for one period of the incoming signal. In the frequency mode, the count gate passes the incoming signal for one period of the oscillator signal.

The period selection is accomplished by using a dual J-K flip-flop connected as shown in Figure 6. The initial state is preset (during the reset cycle) so that the Q outputs of both devices are in the low state. The first negative transition of the incoming signal causes Q_A to go high. The second negative transition causes Q_A to go low, which in turn causes Q_B to go high. Q_B's high is passed by the two series connected NOR gates to the direct clear of A (C_{DA}), which inhibits any further transitions until the devices are reset. As can be observed, the high condition of the Q out-

put of flip-flop A exists only during one complete period of the input to the period selector. This high state is inverted and becomes the gate timing signal.

At first glance it appears that the $\overline{Q}_A$ output could be used directly and eliminate the need for the inversion. However, an MRTL J-K flip-flop behaves in the following way: As the toggle input is clocked, the negative transitions actually cause the $\overline{Q}$ output when high, to attempt to go low. Since the direct clear is held high, $\overline{Q}$ immediately returns to the high state. Consequently, the $\overline{Q}$ output will produce a negative spike at each negative transition of the toggle input. On the other hand, a high on the direct clear insures that the Q output remains low during the toggle input transitions. Therefore, it is desirable to use the Q output and invert, rather than cope with the negative spikes on the $\overline{Q}$ output.

During the normal operating sequence of the period selector, C_{DB} must be kept low and C_{DA} must be connected to Q_B. In order to reset the selector, both C_{DA} and C_{DB} must go high. A DPDT switch could perform this function, were it not for contact bounce. This problem is further discussed in the Manual Reset section. The use of the gating arrangement rather than a switch will then become clear.

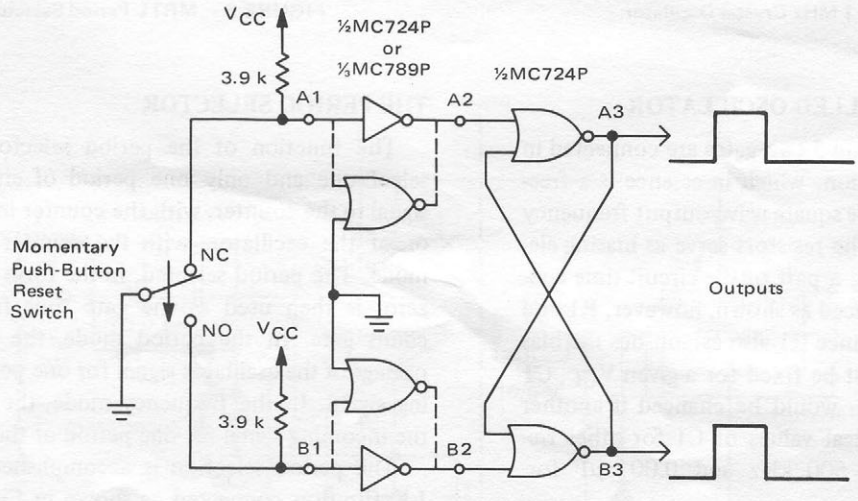
THE MANUAL RESET

The counter is reset by setting the Q outputs of all flip-flops to the low state. This is accomplished by making all direct clears high. Here, a simple switch is inefficient, because if contact bounce is present, malfunctioning results. Some methods have been proposed in the technical literature of rendering the contact bounce non-critical by the use of RC networks. These methods generally depend on making the time constant longer than the duration of the contact bouncing. However, unwieldy values of capacitance are required and usually conflict with device rise and fall time constraints.

The circuit used herein is completely independent of the duration of contact bounce, and meets all constraints of the devices being used. It is, in essence, a bistable multivibrator or, if you prefer, an R-S flip-flop. Figure 7, with its accompanying table, illustrates the various high and low states of the possible switch conditions. As the table shows, once the switch arm makes contact with either the normally closed (NC) contact, or the normally open (NO) contact, no amount of bounce can change the state of the output. The only restriction for the switch arm is that it cannot rebound completely between the NC and NO contact. (Switches of this variety could be called choppers or vibrators.) As in a true switch action, this arrangement yields the complimentary output, either a momentary ON or OFF condition. In this system, unused sections of quad gates are used in the switch to perform the necessary inversion. For this purpose, gates, buffers, or inverters can be used.

THE ONE SHOT MULTIVIBRATOR

As explained in the system discussion, the one shot maintains the reset pulse for 5 μs to insure complete reset. Figure 8 illustrates the one shot configuration of two MRTL NOR gates and only one resistor and capacitor. In a quiescent condition, prior to an input pulse, a steady current flows through R applying a high voltage level or logical "1" to B1. This results in a logical "0" at B3



Switch Status	A1	A2	A3	B1	B2	B3
NC Contact	0	1	0	1	0	1
Interim Bounce After NC Contact	1	0	0	1	0	1
NO Contact	1	0	1	0	1	0
Interim Bounce After NO Contact	1	0	1	1	0	0

FIGURE 7 – MRTL Manual Reset Function.

which is fed back to input A2. Since both A inputs are at a logical "0" at this time, A3 is at a logical "1" level. There is little charge stored in C since both plates are at about the same potential.

If a positive going pulse (logical "0" to logical "1") is now applied to input A1, A3 goes low and C begins to charge. The high initial charging current through R drops the voltage at B1 to a logical "0" that, together with the permanent "0" at B2, switches output B3 to a logical "1". This "1" is fed back to input A2 and maintains A3 at a low level until C charges to the point where B1 reaches the logical "1" threshold level. Then output B3 is switched to a "0" completing the generation of the monopulse. The "0" at B3 is fed back to A2 and the one shot has returned to its original quiescent state.

The presence of this feedback loop makes the duration of the one shot output relatively independent from the duration of the trigger input. It insures that the output of gate A will remain a "0" after the trigger input has reverted to a "0". Thus the duration of the "1" output from the one shot is determined by the value of R and C, not the time duration of the trigger.

The minimum pulse width of the trigger input is governed by the propagation delays of the gates used, and is approximately equal to the sum of the individual propagation delays. Using the MC724P, which typically has delays of 12 nanoseconds, the minimum trigger width would be 24 nanoseconds. The minimum trigger pulse amplitude is, of course, V_{BOT} or 1.8 V Peak. V_{BOT} is the high value voltage applied to an input of an MRTL device to insure saturation of the driven transistor.

The output pulse width, t_d, is determined by the relationship $t_d \approx 0.69$ RC. A pulse width of 225 milliseconds is obtained, using R = 4.3 kΩ and C = 75 μF. There is a recommended maximum value of R that is determined by the relationship

$$R_{max} = \frac{V_{CC} - V_{on}}{I_{in}}$$

For the MC724P,

$$R_{max} = \frac{(3.6) - (0.865)}{0.5 \times 10^{-3}}$$

$$= 5.4\ k\Omega$$

This is necessary, because in the quiescent state sufficient current (I_{in}) must be supplied to gate B to insure its "on" condition.

Variations of the output pulse width were found to be less than ±2% over the +15°C to +55°C temperature range, with pulse widths from 50 μs to 250 μs. The temperature analyses were conducted with the timing R and C outside of the test chamber.

An analysis of the one shot output pulse shows an exponential decay to about the 1 volt level which then falls quite rapidly to the zero volt level. This is due to the exponential voltage rise at B1 as the capacitor C charges. Once gate B starts to switch, the feedback loop provides regeneration and causes the change to be completed abruptly. The output level at which the abrupt change begins is a function of the input threshold voltage and varies from device to device.

A normal question that rises concerning a one shot multivibrator is, will its output pulse drive a flip-flop directly? The MRTL devices in this counter require an input clock pulse fall time in the 10 to 100 ns range and the fall times for one shot output pulse widths less than 5 μs unquestionably meet this constraint. However, while an output pulse width of 225 milliseconds operates a flip-flop to a good confidence level, the buffer conditioning of the one shot output signal assures the resetting of the necessary flip-flops.

One final point to note is that, by removing the feedback loop and grounding A2, the circuit becomes a pulse shortener. Here, the width of the output is dependent only on the value of C.

THE DECADE COUNTING UNIT

In this counter a decade counting unit (DCU) is a device which contains a divide by ten counter, a BCD-to-decimal decoder and a numerical readout.

As shown in Figure 9, the divide-by-ten function is accomplished very simply by using the Motorola MC780P decade counter. The output of the MC780P is a 1, 2, 4, 8 binary coded decimal representation.

Although not new, the most inexpensive way of performing the decoding and readout function is by using the current summing technique. Here, the outputs of the MC780P are used to control the on-off condition of four transistors. The collectors resistors values form a sequence in which each is twice the preceding, resulting in binary weighted collector currents. The currents are brought to a summing junction and since the aggregate current can be in only one of ten discrete states, it is readily displayed on a current meter with a zero through nine scale. An accumulative error of even ±0.25 mA still allows plainly discernable readings. For best results, however, 1% precision resistors are recommended for the current weighting. Carbon film precisions can be purchased reasonably at around 50 cents in single quantities.

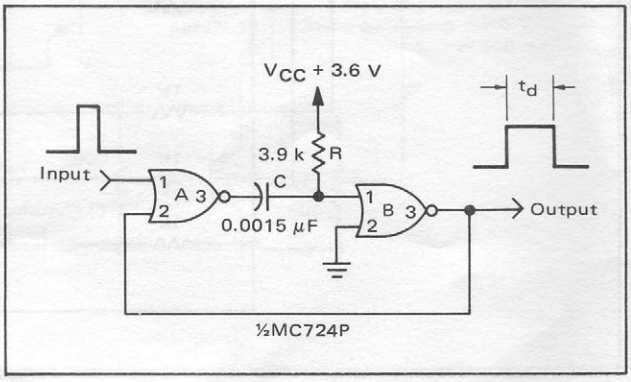


FIGURE 8 – MRTL One Shot Multivibrator.

It might be noted that the values of the collector resistors are not exact binary multiples. This is due to two factors: standard resistors aren't made in the sizes needed and allowance must be made for a variation in the voltage drop across various meters. The resistor values chosen provide more than 10 ma to the meter. This allows shunting of the movement to compensate for meter variations. A modification of the readout mechanism to a neon one-of-ten indicator is contained in AN-514, Figure 9.

THE POWER SUPPLY

The power supply of Figure 10 is a series regulated, emitter referenced, dual output voltage configuration. The voltages are individually adjustable. The range of the nominal 6 V section is 1 V to 6 V, with ±1% regulation to 100 mA. The range of the nominal 3.6 V section is 1.5 V to 6 V, with ±2% regulation to 500 mA at the 3.6 V level. Ripple is 0.2% at full load for the 6 V section, and 1.0% at full load for the 3.6 V section.

SWITCH FUNCTIONS

The 50 to 300 mV/ > 300 mV input sensitivity switch selects the most beneficial input impedance and protection for the two positions provided.

The input frequency range switch divides input frequencies into two ranges. The F position permits measurement over the 10 Hz to 4 MHz range. The F/10 position causes the input frequency to be divided by ten, extending the range by almost an order of magnitude - from 4 Hz to 20 MHz. An MC838P DTL decade counter is used to divide the input frequency by ten, as shown in Figure 11, and imposes the requirement of a 1 μs input fall time for toggle operation. This constraint and input signal rise time determine the minimum operating frequency of the counter. The maximum operating frequency is also determined by the MC838P which is guaranteed only to 20 MHz.

The operate/calibrate switch allows switching from the input to the pulse shaper, to the 120 Hz line frequency for the rough calibration check of ±0.1%.

The frequency/period switch selects the mode of operation. Essentially it interchanges the input signal and the internal oscillator signal routing to the count gate inputs.

The period/period ÷ 10 switch provides a reduced frequency clock signal to the D.C.U.'s to allow the longer periods to be read without over-ranging the readout.

The frequency/period multiplier and gate time switch provides decade ranging for both frequency and period measurements, selects the gate times for random pulse counting, and establishes the recycle time in the automatic reset mode.

The auto/manual switch selects the input signal sampling mode. The manual reset button is a momentary push button which resets and recycles the input signal sampling manually. The on/off switch is self-explanatory.

CONCLUSION

This report describes the complete implementation of a most useful instrument, which can be constructed at minimal cost, and is simple to understand and operate.

Figure 11 is the complete system schematic diagram. Figures 12, 13 and 14 are photographs of the prototype unit.

While the major advantage of this instrument is low cost, an outstanding feature is the use of actual digital

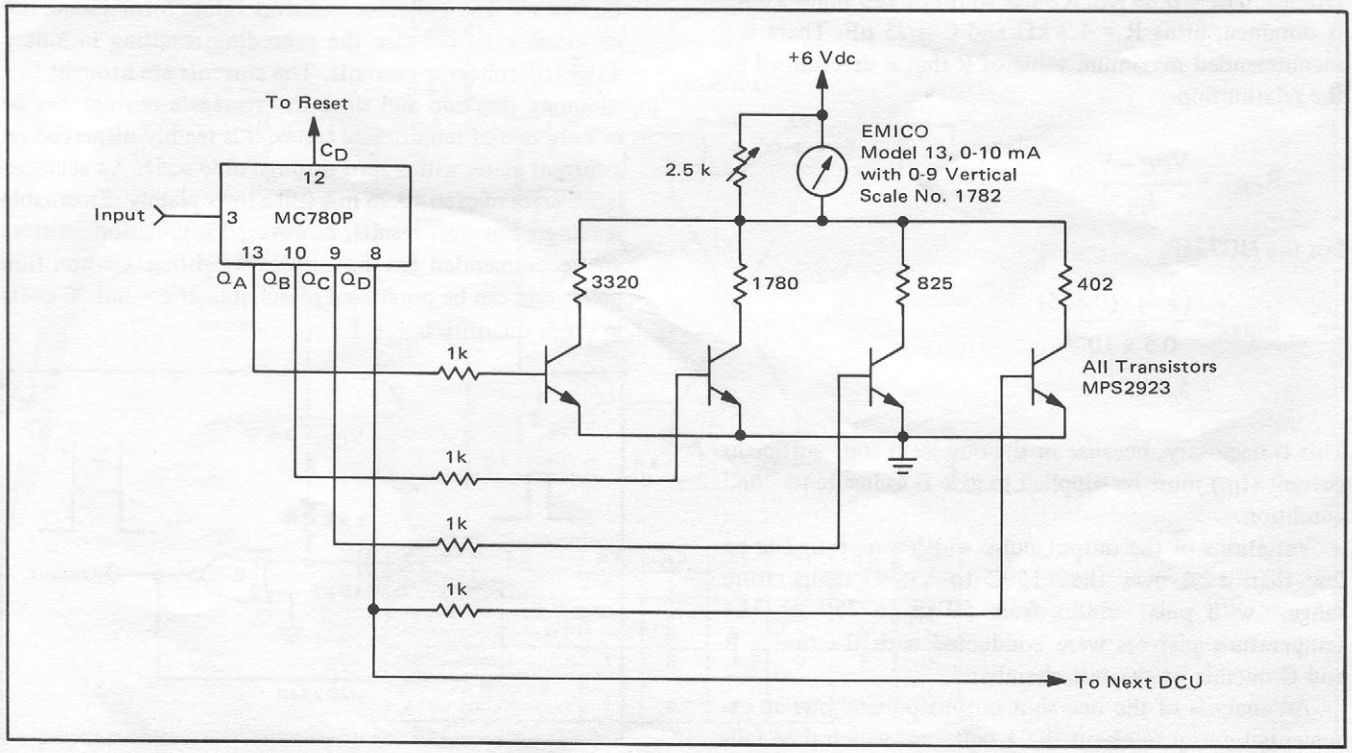


FIGURE 9 – Decade Counting Unit.

devices in performing the many varied functions. This approach yields distinct advantages over the use of discrete devices. Integrated circuits greatly simplify mounting and wiring, especially today because of the multifunction devices available. There is almost no need for level translation or capacitive coupling since the circuits, aside from the logical functions, are composed of devices from the same logic line.

A small disadvantage of the counter is its display which is not read as easily as the familiar neon type numerical tubes. However, when the cost of an entire D.C.U. is considered - less than $10 - the disadvantage shrinks accordingly.

Since devices are "cheaper by the dozen", an engineer dealing with an MDTL or MECL system might construct the counter by implementing the auxilliary functions using devices from the system device family. Figure 15 shows how the counter functions might be realized using MDTL or MECL devices. These and many other circuit functions can be built with "digital" devices. For instance, a logical next step would be to modify the counter's front end so that additional circuit parameters can be measured. The addition of a voltage controlled oscillator would convert the counter to a digital voltmeter resulting in a truly versatile instrument.

ACKNOWLEDGEMENT

The author wishes to acknowledge the technical assistance of William T. Morgan in the preparation of this note and the development of the prototype.

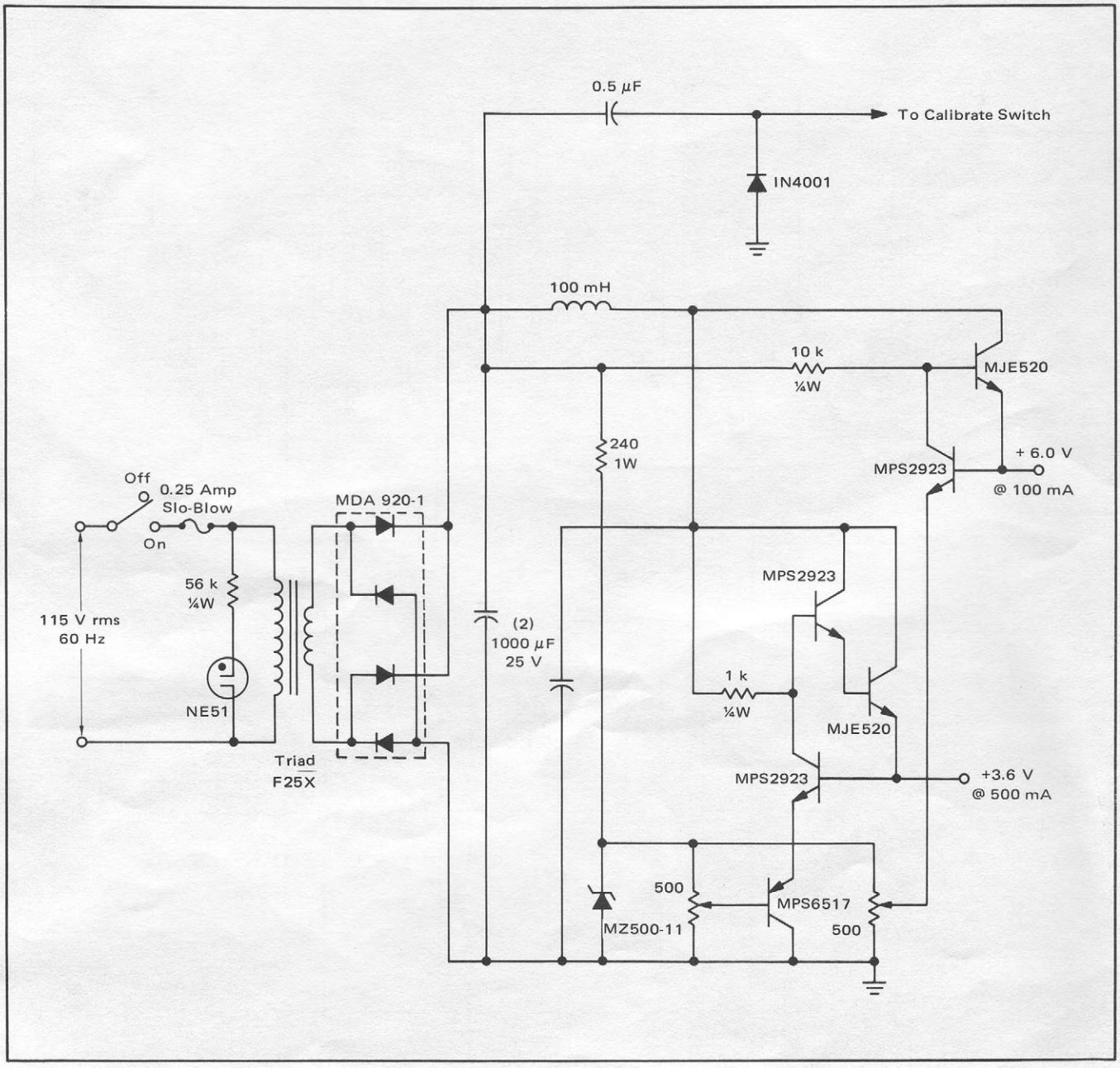


FIGURE 10 – Power Supply.

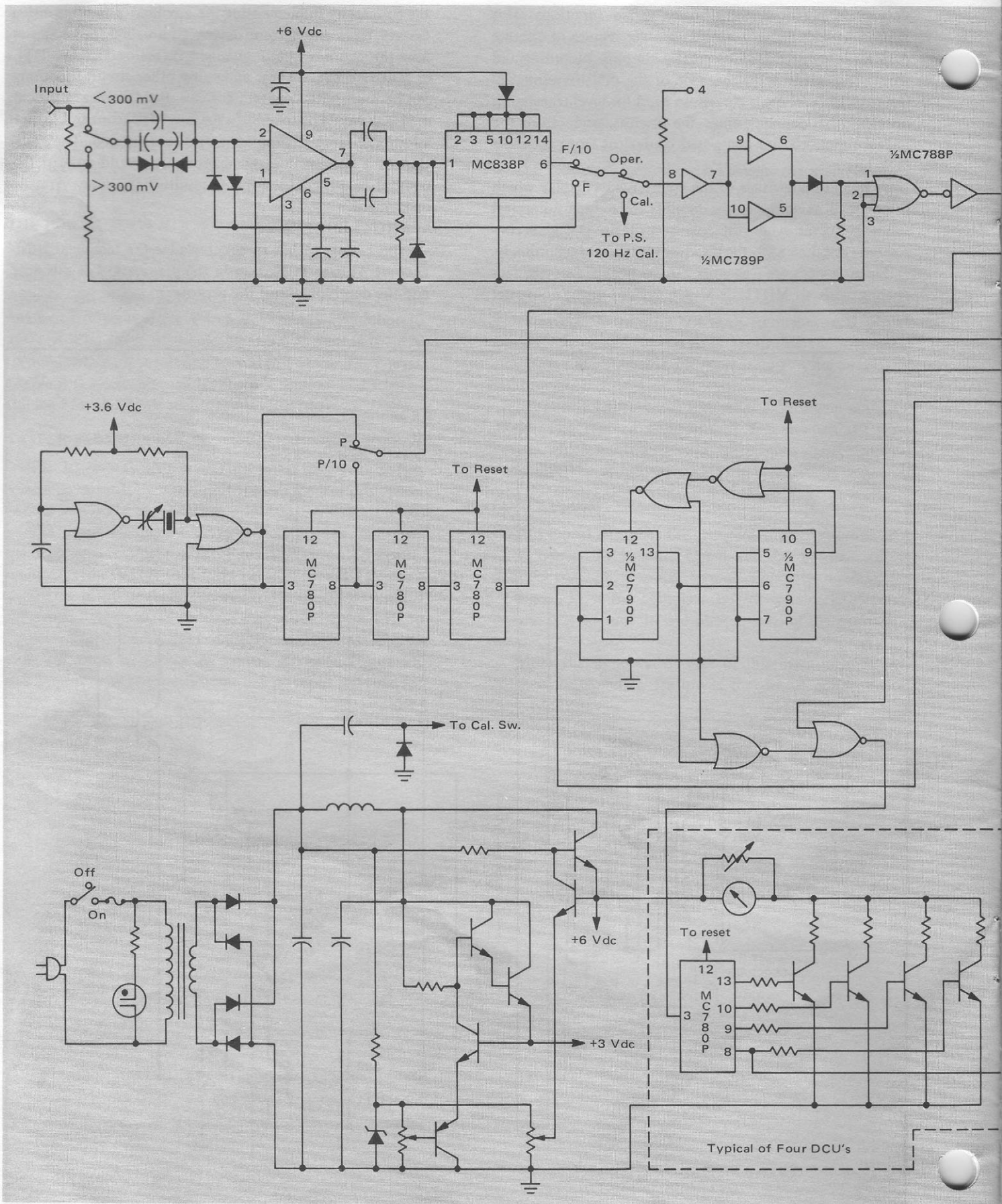
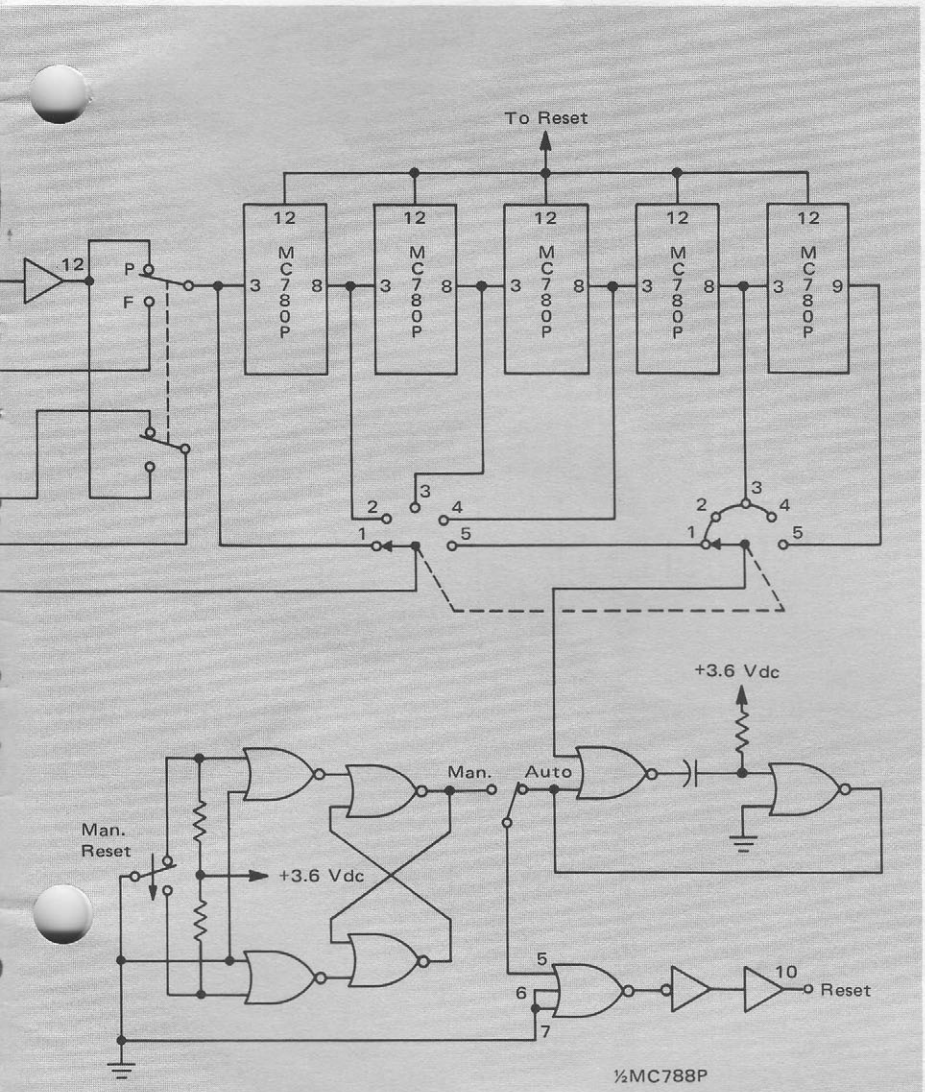


FIGURE 11 – System Schematic 20 MHz Counter.



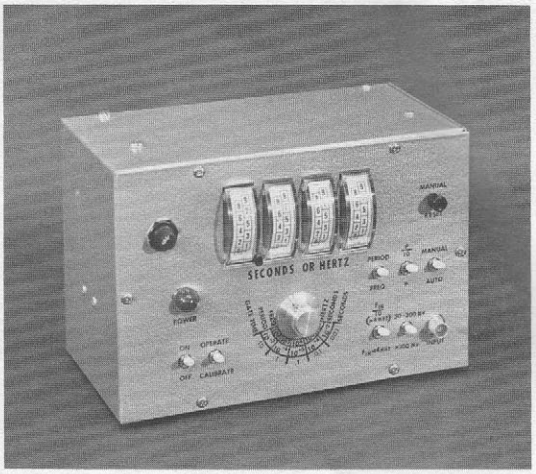


FIGURE 12 – Front View of Complete Instrument

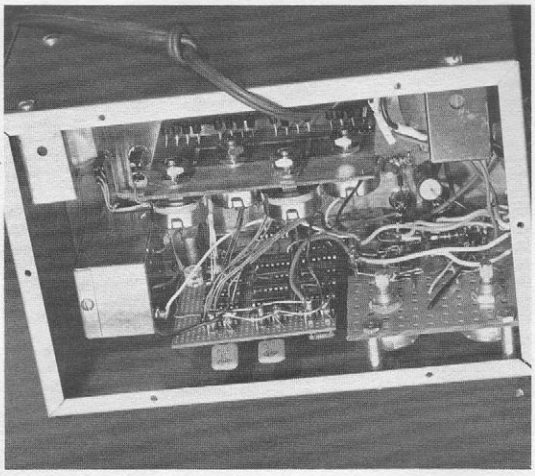


FIGURE 13 – Rear View, from Above

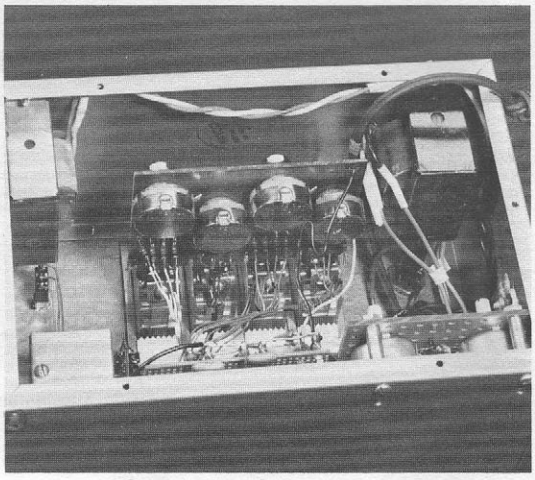


FIGURE 14 – Rear View, from Below

NOTES:
1. For all MRTL devices - Pin 11 is to +3.6 Vdc and Pin 4 is GND, unless otherwise noted.
2. All gates are ¼MC724P unless otherwise noted.
3. Unused Pins (1, 2, 5, 6, 7 & 14) of ALL MC780P devices may be used as isolated wiring terminals.
4. I/C Power Supply Terminals should be decoupled or bypassed with .01 μF capacitors as required. to prevent spurious oscillations.

To Next DCU

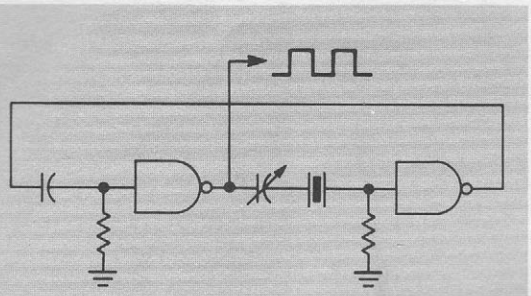
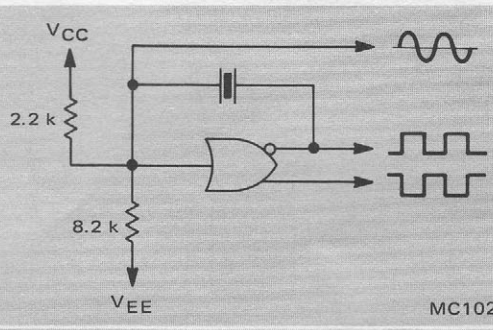
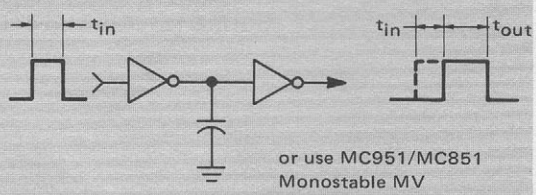
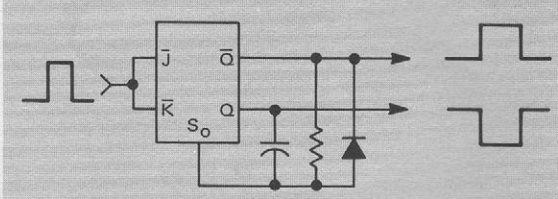
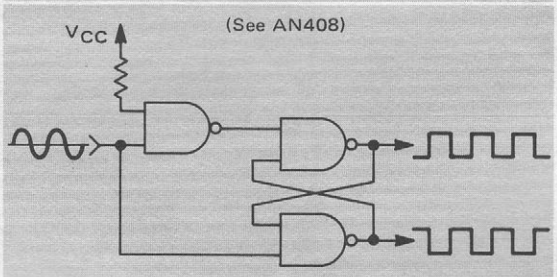
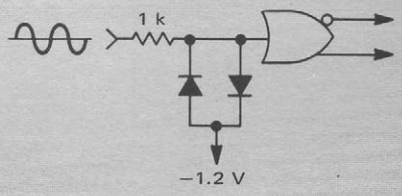
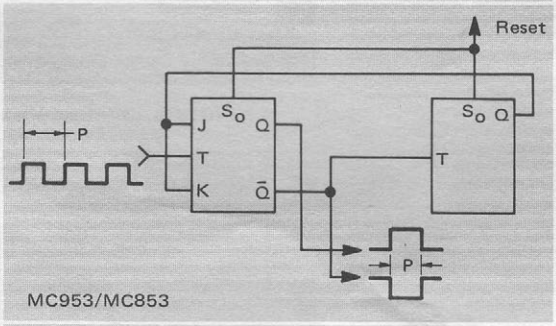
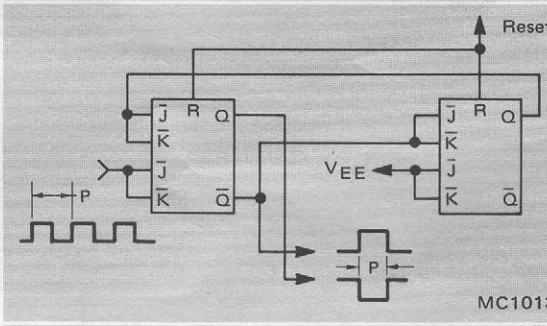
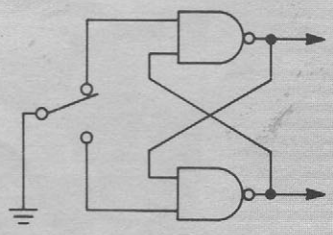
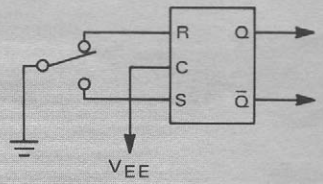
FUNCTION	MDTL	MECL
Crystal Oscillator	 ½MC846	 MC1023
Monostable MV	(See AN409)  or use MC951/MC851 Monostable MV 1/3MC834	(See AN233)  MC1013
Pulse Shaper	 (See AN408) ¼MC846	(For Schmitt Triggers See AN239)  MC1004
Period Selector	 MC953/MC853	 MC1013
Switch Contact Bounce Eliminator	 ½MC846	 ½MC1015

FIGURE 15 – MDTL and MECL Implementation of Various Circuit Functions Used in the Frequency/Period Counter.

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